TOWARDS LOW NOISE, HIGH POWER AND EFFICIENCY MM-WAVE AND TERAHERTZ CIRCUIT DESIGN

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Mm-wave and terahertz frequency range is gaining vast attention in recent years due to attractive applications in various areas including spectroscopy, imaging, security and high data-rare communication. All these systems require high performance circuits for power generation and amplification. In recent years, many amplifiers and oscillators have been fabricated in SiGe and CMOS processes to show the feasibility of implementing these systems in this frequency range. Despite all the efforts and ideas employed to enhance the performance of these blocks, there is still a long way to go to achieve reasonably high performance amplifiers and signal sources at mm-wave and terahertz frequencies. The main challenge comes from the activity degradation of the transistors, high loss in the passives and high noise in the active and passive devices at this frequency range. In this work, new systematic design methods for low noise and high gain amplifiers and high power and efficiency oscillators at mm-wave and terahertz frequencies are presented.

Chapter 1 reviews the basic concepts of the two-port networks such as stability, activity, power gains and noise parameters. These subjects are vastly used in the next chapters of this work when presenting the new methods for high frequency circuit design.

In chapter 2, a new convex stability region is presented based on which, a systemic amplifier design method beyond $f_{max}/2$ is proposed which moves the network toward the high gain region using optimum passive embeddings. This method is capable of

considering modeling errors of the components during the design process which results in a robust, stable and high gain amplifier. Employing this method, a three stage amplifier working at 173 GHz is designed and implemented in a 130 nm SiGe process which shows 18.5 dB gain, 8.2 GHz 3-dB bandwidth and 0.9 dBm saturated output power in the measurement. A new FoM is defined to fairly compare different amplifiers fabricated in different processes which targets the capability of the design method in extracting the power amplification potential of the active device. This amplifier achieves the highest FoM among all reported state of the arts works above $f_{max}/2$ in SiGe/CMOS processes which shows the efficacy of the proposed method in fully utilizing the process capabilities in amplifier design.

In chapter 3, high frequency LNA is targeted and a systematic method to design low noise and high gain amplifier beyond $f_T/2$ is presented. To achieve this goal, noise measure of the proposed structure becomes minimum employing optimum passive embeddings while the stability of the circuit is assured using the convex stability region derived in chapter 2. The guidelines and required noise and power equations to complete the systematic LNA design are derived and presented in this chapter. Employing this method, a 91 GHz LNA with 5.6 dB noise figure, 9.7 dB gain and 6.3 mW dc power consumption is implements in a 130 nm SiGe process. Comparing these results with the state of the arts using the proposed FoM that takes the process and power consumption into account justifies the effectiveness of this design method in fully utilizing low noise and high power generation capability of the process.

A design methodology for high power mm-wave VCO design is presented in chapter 4. Using the complete passive embeddings including the load, the power gain from the input of the active device to the load is maximized which results in an oscillator with high power at the output and significantly improved DC-to-RF efficiency. In addition, the proposed structure is capable of providing sufficient tuning range which is

an important factor in mm-wave source design and applications. A VCO working at 110 GHz is designed and implemented in a 55 nm SiGe process employing this method which shows 6.3 dBm peak output power, 20.9% DC-to-RF efficiency and 5.2% tuning range. This VCO achieves highest peak output power in F and D band (90 GHz to 170 GHz) and highest DC-to-RF efficiency in frequencies below $f_{max}/2$ among all reported mm-wave oscillators in SiGe/CMOS processes.

Chapter 5 represents a new design method for high power and efficiency harmonic oscillator. This method exploits different mechanism to enhance the fundamental oscillator performance, increasing the harmonic power generation in the active device and effectively delivering the generated harmonic power to the load using various passive embeddings in a cross-coupled structure. Capacitive degeneration is employed to shape G_m of the structure. Inductive embeddings at the base of the transistors are utilized to provide sufficient voltage gain and increase harmonic current generation in the active device. The embeddings at the collector are used to maximize the output resistance of the structure which results in delivering majority of the generated current to the load. Employing this method, a 300 GHz harmonic oscillator is designed and implemented in a 130 nm SiGe process which shows 2.8 dBm peak output power and 4.5% DC-to-RF efficiency with 86.6 mW/mm^2 power-area efficiency. Also, a harmonic VCO is implemented with 2.3 dBm peak output power, 3.5% DC-to-RF efficiency and 1.5% tuning range and 77.2 mW/mm^2 power-area efficiency in the same process. This harmonic oscillator method significantly improves the power-area efficiency of high frequency signal sources and the designed oscillator achieves the highest power-area efficiency among all reported SiGe/CMOS oscillators working above 0.75 f_{max}.

BIOGRAPHICAL SKETCH

Somayeh Khiyabani received the B.Sc degree in Electrical Engineering from Sharif University of Technology, Tehran, Iran in 2011 and the M.Sc degree in Electrical and Computer Engineering from Cornell University, Ithaca, NY in 2015. She is currently working toward her PhD program in Electrical and Computer Engineering in UNIC research group at Cornell University. Her research in doctoral program is developing systematic methods for optimum mm-wave and THz circuit design including low noise and high power gain mm-wave amplifiers and high output power and efficiency VCO's and harmonic oscillators. In summer 2016, she was an intern at Qualcomm Inc, San Jose, CA working on ultra low power RF receivers. She was also a recipient of Jacobs fellowship at Cornell University in fall 2012.

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CHAPTER 1

BASICS OF LINEAR TWO-PORT NETWORK

A linear two-port network can be fully described by the relation between its input and output currents and voltages at a given frequency and bias point. As shown in Fig. 1.1, assuming $I_1 = I_1^{'}$ and $I_2 = I_2^{'}$, four circuit variables are available to be measured. To represent a two-port network, two of these variables are considered independent and the other two are defined in terms of them. Based on independent variable selection, different matrices are defined for describing the network. One form of the network matrix representation is the admittance matrix, $Y = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}$, in which the currents are defined in terms of the voltages:

$$I_1 = y_{11}V_1 + y_{12}V_2$$
$$I_2 = y_{21}V_1 + y_{22}V_2. \tag{1.1}$$

The admittance matrix elements (y_{ij}) are complex quantities in general and can be written in terms of the real and imaginary parts as $g_{ij} + jb_{ij}$.

The network matrices are very useful in defining important characteristic of the network and their combinations. activity/passivity and stability are among the important

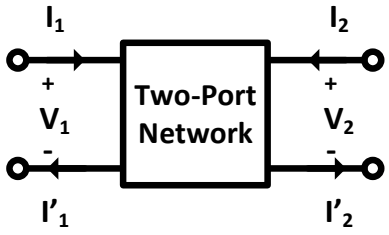

Figure 1.1: A two-port network

features of the two-port networks which have significant role in circuit design are and are discussed in the following.

1.1 Activity and Passivity

The definition of activity/passivity of a network is based on the real signal power generation or consumption by the network. Therefore, it is worthwhile to briefly review the signal power of a two-port network before stating the definition and constraints of activity/passivity.

Using the equations in (1.1) for the two-port network shown in Fig. 1.1, the complex signal power flowing into the network at a given frequency is written as:

$$P = P_R + jP_I = V_1 I_1^* + V_2 I_2^* = y_{11}^* |V_1|^2 + y_{22}^* |V_2|^2 + y_{12}^* V_1 V_2^* + y_{21}^* V_1^* V_2, \tag{1.2}$$

where P_R and P_I are real numbers and are called real signal power and imaginary signal power respectively.

The activity/passivity of a two-port network can be determined by examining the real signal power (P_R). The network is said to be passive at a given frequency if $P_R > 0$, which means the average real power flowing into the network is positive and it is dissipating the power. On the other hand, If $P_R < 0$, the network is active and is generating real power.

It is essential to drive the conditions for activity/passivity of the network in terms of its matrix elements in order to have an insight in the process of circuit design. Using P_R formula derived from (1.2), it can be shown that [1]:

$$\frac{P_R}{|V_1||V_2|} = a^{-1} g_{11} + a g_{22} + |y_{12} + y_{21}^*| \cos(\measuredangle(y_{12} + y_{21}^*) + \alpha), \tag{1.3}$$

where $a = |\frac{V_2}{V_1}|$, $\alpha = \measuredangle \frac{V_2}{V_1}$, $g_{11} = Re(y_{11}^*)$ and $g_{22} = Re(y_{22}^*)$.

Because $|V_1|$ and $|V_2|$ are positive numbers, the sign of this equation is determined by P_R which is directly related to the activity/passivity definition. Therefore, examining the sign of the right hand side term in (1.3) results in the conditions for activity/passivity of the network. If either $g_{11} < 0$ or $g_{22} < 0$, then P_R can be made negative by choosing sufficiently large or small quantity for a. Another possibility of having a negative P_R is assuming positive g_{11} and g_{22} and let the third term in the right-hand side of (1.3) make the sign to be negative. It can be shown that if $4g_{11}g_{22} < |y_{21} + y_{12}^*|^2$ then P_R would be negative [1]. As a result, the passivity conditions of a two-port network are:

$$\begin{aligned} g_{11} &\geq 0 \\ g_{22} &\geq 0 \\ 4g_{11}g_{22} &\geq |y_{21} + y_{12}^*|^2. \end{aligned} \tag{1.4}$$

A two-port network is active if at least one of the above inequalities is not satisfied. It is worth mentioning that these conditions are bias and frequency dependent since the network parameters are defined at a certain bias and frequency.

1.2 Stability

Stability is one of the important characteristic to be considered in amplifier and oscillator design. The designer should make sure of stability of the amplifier whereas ensuring the instability of the oscillator at the desired frequency. The instability of a two-port network at a given frequency is usually defined as having oscillation at either the input or the output ports at that frequency.

A two-port network is said to be ***absolutely stable*** at a given frequency if it does not

oscillate at that frequency in neither input or output ports under any passive termination at those ports. If at least one passive termination causes oscillation at the input or the output at that frequency, the network is ***potentially unstable***. Like activity/passivity, the stability of a two-port network is also frequency and bias dependent. For instance, a two-network can be absolutely stable at one frequency and potentially unstable at an other one. Using the stability definition, i.e. no oscillation at either ports, the conditions of stability can be derived which are known as ***Llewellyn conditions*** [2]:

$$\begin{aligned} g_{11} &\geq 0 \\ g_{22} &\geq 0 \\ 2g_{11}g_{22} - M &\geq L, \end{aligned} \tag{1.5}$$

where $M + jN = y_{12}y_{21}$ and $L = \sqrt{M^2 + N^2}$.

If all the above inequalities are satisfied, the two-port network is absolutely stable at the frequency of interest. If at least one of them is not met then the network is potentially unstable at that frequency. It is worth noting that a potentially unsaleable network does not necessarily oscillate when connected to the desired passive load and source admittances. It simply means that there are one or more passive termination sets that cause oscillation in the network and make it unstable. These terminations should be avoided if the network is supposed to be an amplifier and should be provided if designing an oscillator.

Since in most of the cases the first two inequalities in Llewellyn condition are satisfied, the third one becomes determinant. Starting form that, the well-known stability factor can be derived [1]:

$$\eta = \frac{2g_{11}g_{22} - M}{L}. \tag{1.6}$$

If for a two-port network $\eta \geq 1$, it is absolutely stable in case $g_{11} \geq 0$ and $g_{22} \geq 0$. If

$\eta < 1$ then two-port network is potentially unstable.

As the foregoing discussion shows, the derived condition is for a two-port network which is not terminated. In case of $\eta < 1$, the only information it provides is that there are some passive terminations which cause instability. But one cannot know whether one curtain selection of source and load impedances will cause instability in the given two-port network by examining η unless the y-parameters used in the condition also include these impedances as part of the two-port network. Assuming terminated two-port network in Fig. 1.2, the stability factor that captures the source and load impedances in determining the stability of the network is known as ***Stern's stability factor (k)*** [3]:

$$k = \frac{2(g_{11} + g_S)(g_{22} + g_L)}{L + M}, \tag{1.7}$$

where g_S and g_L are real parts of the source and the load admittances. $k > 1$ corresponds to the stability of the terminated network.

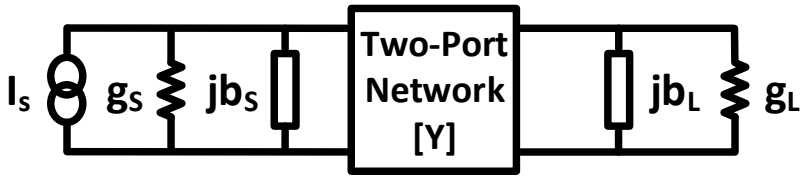

Figure 1.2: Terminated two-port network

It is worthwhile to examine the activity/passivity and the stability relation. Considering the conditions derived for each, one can conclude that passivity always results in absolute stability. Also, activity of a two-port network does not always lead to potential instability. Indeed, it is a necessary but not sufficient condition for potential instability [1].

1.3 Power Gains

In the study of active mm-wave circuits as the two-port networks, one important factor to consider is the power flow. Since these circuits are designed to amplify the power at the desired frequency, it is reasonable to have a measure to characterize it. There are various defined power gains which differ from each other in the quality of the power transfer at the input and the output. Thus, before stating the power gain definitions, the power transfer quality in a two-port network should be explained.

In order to have the maximum power flow to/from a port (P_{av}), the port should be matched to conjugate of its impedance, i.e. $y_{termination} = y^*_{port}$ [4]. Therefore, for maximum power transfer at the input and output of a two-port network at the same time, both of them should be conjugately matched. This network is said to be ***Simultaneously Conjugate-Matched (SCM)***. It can be shown that SCM condition is possible only if the two-port network is absolutely stable ($\eta \geq 1$) at the desired frequency [1].

Assume the terminated two-port network in Fig. 1.3. $P_{av,S}$ and $P_{av,L}$ are the power delivered to and transfered from the input and output respectively in SCM condition and P_{In} and P_L are those powers in general case respectively. Based on this, different power gains can be defined that one of them can be more meaningful and useful depending on the circuit block. Also, deriving these power gains in terms of y-parameters of the network enables the designers to have an insightful design. It is beneficial to briefly review some of them in this section since they will be used in the next chapters.

(a) Operating Power Gain (G_P):

$$G_P = \frac{P_L}{P_{In}} = \frac{|y_{21}|^2 g_L}{|(y_{22} + y_L)|^2 Re(Y_{in})}, \tag{1.8}$$

where $g_L = Re(y_L)$ and Y_{in} is the input admittance of the network.

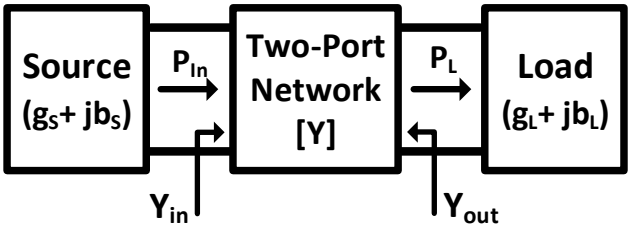

Figure 1.3: Power transfer in a two-port network connected to the source and the load

(b) Transducer Power Gain (G_T) [1]:

$$G_T = \frac{P_L}{P_{av,S}} = \frac{4|y_{21}|^2 g_S g_L}{|(y_{11}+y_S)(y_{22}+y_L)-y_{12}y_{21}|^2}, \tag{1.9}$$

where $g_L = Re(y_L)$ and $g_S = Re(y_S)$. G_T is the most meaningful and practical power gain when the two-port network is designed to be an amplifier since it takes into account the effect of input and output matching quality.

Two useful special case of the power gains are worth mentioning here which are referred to in the rest of this work:

(a) Maximum Transducer Power Gain (G_c): If the two-port network is assumed to be SCM, then G_T reaches to its maximum which is called G_c and can be derived from (1.9) applying SCM conditions as [1]:

$$G_c = G_{T,max} = \frac{|y_{21}|^2}{2g_{11}g_{22}(1+R)-M} = \frac{|A|}{\eta+\sqrt{\eta^2-1}}, \tag{1.10}$$

where $A = \frac{y_{21}}{y_{12}}$ and $R = \sqrt{1-\frac{M}{g_{11}g_{22}}-\frac{N^2}{4g_{11}^2g_{22}^2}}$.

(b) Unilateral Power Gain (U): This power gain is widely used in the literature. It is defined under assumption of an SCM two-port network which is also unilateral, i.e. $Y_{12} = 0$ where Y_{12} is the y-parameter of the embedded network, and can be written

as [5]:

$$U = \frac{|y_{21} - y_{12}|^2}{4(g_{11}g_{22} - g_{12}g_{21})}. \tag{1.11}$$

In addition to be a power gain, U has some other unique features. The most important and useful one is that it remains invariant under four-port, linear, lossless and reciprocal passive embeddings [6]. This characteristic is utilized in the next section when defining the stability boundary and the gain plane. Another significant characteristic of U is that it can be considered as the activity/passivity criterion of a two-port network. It is straight forward to show that the third inequality in (1.4) is equivalent to $U \leq 1$ [1]. Therefore, $U > 1$ indicates that the network is active at the given bias and frequency.

1.4 Noise in Two-Port Networks

A noisy linear two-port network can be modeled by the original noiseless two-port network and two additional noise sources [7]. In general, these two noise sources are correlated that means four parameters (the two noise sources and the real and imaginary parts of the correlation factor) should be known to fully describe the noise behavior of the network. There are six possibility of representing a noisy two-port network depending on the type of the added noise sources and the nodes to which they are connected [8]. The most common model which is convenient to use in noise analysis of two-port networks is shown in Fig. 1.4. The noisy two-port network is modeled by the noiseless network and the correlated input referred voltage and current noise sources. Noise is a random process and its average power is utilized in noise analysis of the circuits. Therefore, the noise sources are usually referring to the average power of the noise, $\overline{V_n^2}$ and $\overline{I_n^2}$, as shown in Fig. 1.4.

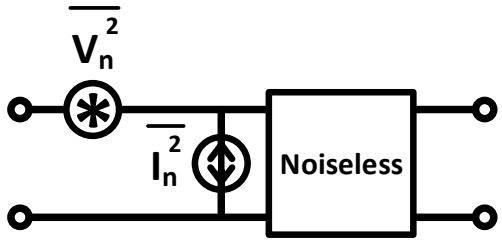

Figure 1.4: Representing a noisy two-port network by the original noiseless network and two correlated noise power sources at the input

In order to calculate the correlation between the noise sources, the model in Fig. 1.4 can be replotted as Fig. 1.5. The noise current is divided into correlated and uncorrelated parts and can be written as:

$$I_n = I_u + I_{cor} = I_u + Y_{cor} V_n \tag{1.12}$$

where I_u is the uncorrelated current noise and I_{cor} is the correlated one. Multiplying each side by V_n^* results in the correlation admittance [9]:

$$Y_{cor} = \frac{\overline{I_n V_n^*}}{\overline{V_n^2}} = G_{cor} + jB_{cor}. \tag{1.13}$$

I_n, V_n, G_{cor} and B_{cor} model the noisy two-port completely.

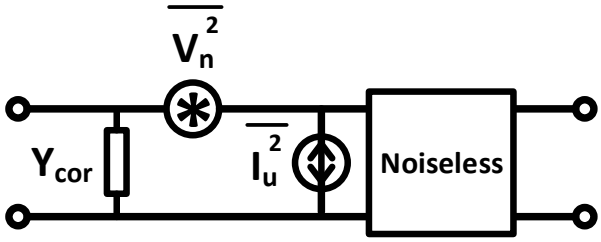

Figure 1.5: Representing a noisy two-port network capturing correlation admittance

The dual of this model also can be helpful in some noise analysis in which V_n is modeled with an uncorrelated noise source and a correlation impedance (Z_{cor}) with respect to I_n as shown in Fig. 1.6. In this case, I_n, V_n, R_{cor} and X_{cor} fully describe the noisy two-port where $Z_{cor} = R_{cor} + jX_{cor}$.

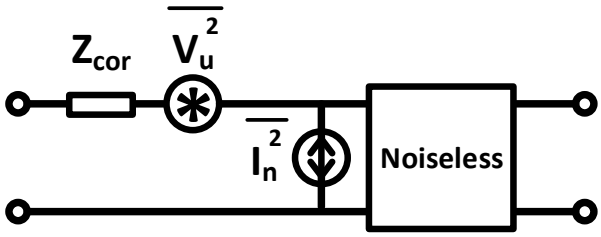

Figure 1.6: Representing a noisy two-port network capturing correlation impedance

The noise of a two-port network is an important factor in the certain circuits like LNAs' since it can increase the overall noise of the system significantly and worsen the detection of the signal. Hence, a reasonable measure is required to formulate this effect and provide some insight toward the design.

The specification that shows the contribution of the noise of two-port network in the total noise of the system is ***Noise Factor (F)***. Assume the noisy two-port network is connected to a noisy source as shown in Fig. 1.7. The noise factor is defined as [10]:

$$\text{Noise Factor} = \frac{\text{Total Output Noise Power}}{\text{Output Noise Power due to the Input Noise}} = \frac{\text{SNR}_{\text{in}}}{\text{SNR}_{\text{out}}}. \qquad (1.14)$$

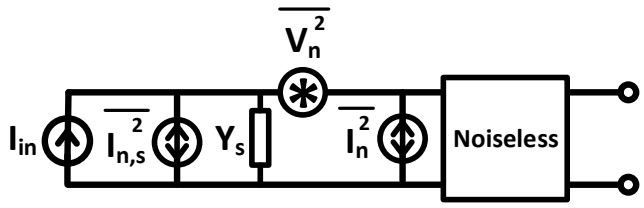

Figure 1.7: A noisy two-port network connected to a noisy source

In the literature, it is most common to report F in dB. This parameter is called ***Noise Figure*** *(NF)* and is defined as $10\log(F)$. As it is evident from the definition in (1.14), if two-port network is noiseless, then $F = 1$ and if it is noisy, $F > 1$. Therefore, the measure to examine how much the noise of the two-port network adds to the noise at the output is to compare its F to 1 or equivalently NF to 0 dB (noiseless condition). It is also noteworthy that F is a per Hertz quantity and to find the total noise power in a certain frequency range, it should be integrated across the desired bandwidth.

It is helpful to derive F in terms of network parameters in order to have insight in the design process to achieve low F. To do so, assume the noisy two-port network connected to a noisy source shown in Fig. 1.7. Since the noiseless two-port network and the output termination are common for all noise sources at the input and will be canceled out considering the definition of F, they can be assume as a simple wire and the model to work on would be reduced to Fig. 1.8. Using the definition of F one can derive [11]:

$$F = \frac{\overline{I_{out,tot}^2}}{\overline{I_{out,s}^2}} = \frac{|I_{n,s} + I_u + (Y_s + Y_{cor})V_n|^2}{|I_{n,s}|^2}. \tag{1.15}$$

Equation (1.15) can be written in terms of noise, correlation and source admittances which is more helpful to utilize in the design process. Assuming $\overline{I_u^2} = 4KTG_u\Delta f$,

$\overline{I_{n,s}^2} = 4KTG_s\Delta f$ and $\overline{V_n^2} = 4KTR_n\Delta f$, the new form of F is:

$$F = 1 + \frac{G_u + |Y_s + Y_{cor}|^2 R_n}{G_s} = 1 + \frac{G_u + R_n[(G_s + G_{cor})^2 + (B_s + B_{cor})^2]}{G_s}, \qquad (1.16)$$

where G_i and B_i are real and imaginary parts of Y_i.

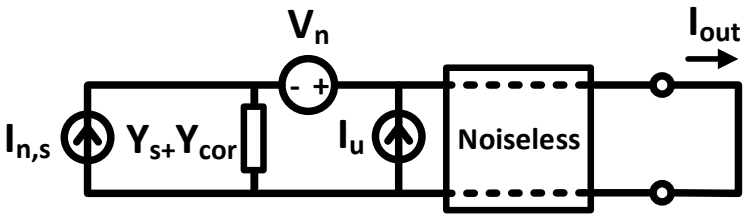

Figure 1.8: Tow-port model for calculating noise factor (F)

Since F is expressed as a function of the source admittance in (1.16), it is advantageous to find the optimum value of Y_s that yields to the minimum F. Indeed, this procedure results in the minimum input noise transfer to the two-port and can be considered as ***noise matching*** compared to the power matching that proper admittance value is found to have the maximum power transfer. The ***optimum source admittance*** is achieved by taking derivative from (1.16) in terms of G_s and B_s and equating them to zero [11]:

$$G_{s,opt} = \sqrt{G_{cor}^2 + \frac{G_u}{R_n}} \quad , \quad B_{s,opt} = -B_{cor}. \qquad (1.17)$$

Substituting this values into (1.16) results in the minimum F:

$$F_{min} = 1 + 2R_n(G_{cor} + G_{s,opt}). \qquad (1.18)$$

The same method can be applied to the model with correlated impedance (Z_{cor}) and the ***optimum source impedance*** is derived as:

$$R_{s,opt} = \sqrt{R_{cor}^2 + \frac{R_u}{G_n}} \quad , \quad X_{s,opt} = -X_{cor}, \qquad (1.19)$$

where $G_n = \frac{\overline{I_n^2}}{4KT\Delta f}$ and $R_u = \frac{\overline{V_u^2}}{4KT\Delta f}$.

It is worth mentioning that if $Y_{in}^* \neq G_{s,opt} + jB_{s,opt}$ where Y_{in} is the input admittance of the two-port network, then there is a trade-off between noise and power matching. The general noise factor in (1.16) can be rewritten as:

$$F = F_{min} + \frac{R_n}{G_s}[(G_s - G_{s,opt})^2 + (B_s - B_{s,opt})^2]. \tag{1.20}$$

This is a useful equation which shows how the quality of the noise matching and also the noise of the two-port network affect F and deviate it from the desired F_{min}. Figure 1.9 conceptually depicts the constant F circles derived in (1.20) in $G_s - B_s$ plane.

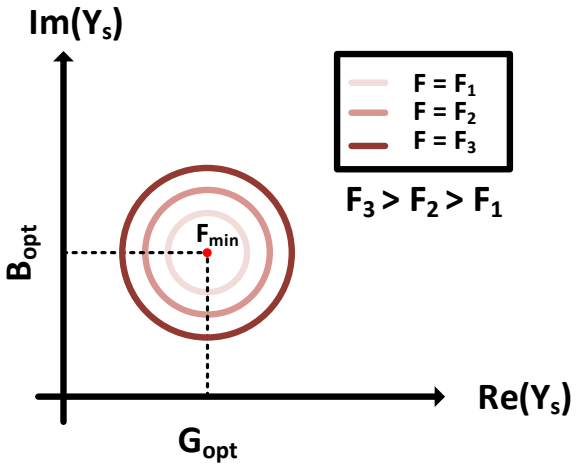

Figure 1.9: Demonstration of noise factor (F) and noise matching in $G_s - B_s$ plane

The last subject to cover in this chapter is the total noise factor of a chain of noisy two-port networks (F_{tot}). It is a practical case since in reality different circuits are cascaded to achieve the desired performance. Assume a chain of N cascaded networks in which the network i has F_i and $G_{c,i}$ as the noise factor and maximum transducer power gain as shown in Fig. 1.10. It can be shown that the total noise factor of this chain can

be written as [10]:

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_{c,1}} + \frac{F_3 - 1}{G_{c,1}G_{c,2}} + ... + \frac{F_N - 1}{G_{c,1}G_{c,2}...G_{c,N-1}} \tag{1.21}$$

where F_i is calculated with respect to the previous stage output resistance ($R_{out,i-1}$). This equation is known as ***Friis' Equation*** and shows that the noise factor of the first stage in the chain is the most important one in determining the overall noise factor of the system when having cascaded gain stages.

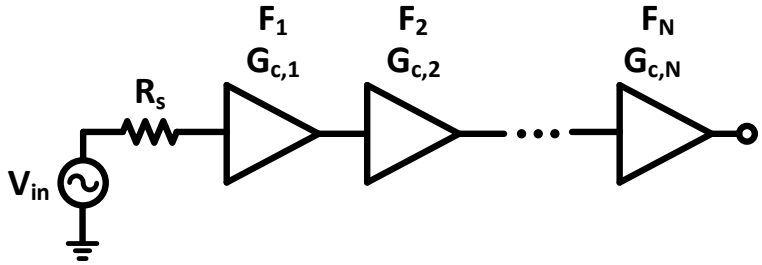

Figure 1.10: Chain of cascaded noisy two-port networks connected to the source

CHAPTER 2

A SYSTEMATIC DESIGN OF HIGH-GAIN AMPLIFIERS ABOVE $F_{MAX}/2$

2.1 Introduction

Millimeter-wave (mm-wave) and terahertz (THz) systems promise many attractive applications in different areas [12–18]. However, there are many challenges toward the implementation of these systems. In particular, the passive components are more lossy in these frequency ranges due to the skin effect and also operating close to their self-resonance frequency. Thus, it is vital to design amplifiers with decent power gain in these frequency ranges. More importantly, as frequency approaches the f_{max}, the activity of the device decreases and hence its ability for power generation and amplification degrades [1, 19]. Therefore, high power generation and/or high power gain at high frequencies is a hard goal to achieve. The degradation of activity can be observed by studying the unilateral power gain of the device (U), which is the activity Figure of Merit (FoM) [6]. U decreases by a slope of 20 dB/dec above the $f_{max}/2$ [20], and reaches 0 dB at f_{max}, beyond which the device is no longer capable of power amplification/generation. In addition to its invariance which makes it an inherent value of a two-port network, the importance of U stems from the fact that the maximum transducer power gain (G_C) of a stable two-port network (which is the most practical and useful measure of power gain [4]), is limited by $(\sqrt{U} + \sqrt{U-1})^2$ [1].

There is a trade-off between the power gain and stability. Since solid-state circuits are strongly affected by many types of variations, being too close to the stability boundary without considering the potential errors and variations is quite risky and it is possible that the fabricated circuit has a poor power gain or becomes unstable and hence either oscillates or saturates independent of the input signal [1]. In addition, the real part of the

input impedance and/or output impedance diminishes by getting closer to the stability boundary, which results in a more lousy and lossy matching network. A lossy matching network can provide conjugate matching merely from one side and hence degrades the transducer power gain both by its loss and by its incomplete matching.

In recent years, researchers have tried to come up with new methods to overcome the challenges in mm-wave and THz power amplification. As a first step, there has been an ongoing research in the device fabrication technologies in order to increase f_{max} [21]. Others have tried to carefully design the amplifiers and their matching networks to achieve higher power gain from each employed device [22–24].

To the best of our knowledge, the only systematic approach to design a mm-wave amplifier is the so-called unilateralization [5, 25–30]. The main idea in this method is to eliminate the reverse signal path from the output to the input. In this case, the maximum transducer power gain becomes equal to the unilateral power gain of the circuit ($G_C = U$). A unilateralized device not only usually has a better power gain than the original device, but also becomes stable and SCM would be possible. An internal unilateralization technique is introduced in [27] and verified by implementing a 50 GHz amplifier with 20 dB power gain. A transformer based feedback for unilateralization is proposed in [28] and an amplifier working at 46 GHz with 18.3 dB power gain is fabricated. A unilateralization method is employed in [30] to design an amplifier with 22.5 dB power gain at 233 GHz. However, none of these works achieved a power gain of more than $0.51 \times U$ which can be explained by the loss of passives and matching networks and more importantly it is due to variations and modeling errors. Although unilateralization is used in amplifier design, it suffers from four major issues. The first and the foremost important one is that this method results in wasting the capability of the transistor which is able to produce higher power gain ($(\sqrt{U} + \sqrt{U-1})^2$) than what

targeted (U). The second issue is that the elimination of the reverse path to the input is usually narrow band and hence the bandwidth of the resulting amplifier is very limited. Third, none of the proposed methods of unilateralization are capable of considering the corners and variations of the components which results in much lower gain than expected ($0.51 \times U$ at best which is achieved by [30]). Finally, at the design stage, all the suggested methods assume that the passives are lossless which is an unreasonable assumption at high frequencies.

There is a heuristic approach whose results are closer to unilateralized power gain compared to the works where unilateralization has been targeted [1, 31]. This approach maximizes a power related function in order to achieve a high power gain. In fact, instead of the power gain, the real part of $(P_{out} - P_{in})/(|V_{in}V_{out}|)$ is maximized, which means there is no guarantee that this method can always result in a reasonable power gain. Besides, it is never possible to guarantee the optimality conditions in this method. In particular, it demands for a constant phase shift and voltage gain across the device, none of which can be easily satisfied in an amplifier. Besides, the optimality conditions demand for a constant phase shift and voltage gain across the device, none of which can be easily satisfied in an amplifier. The amplifier is designed using sweeping tool in Cadence and does not satisfy any of the optimality conditions.

In this paper, a novel stability region is derived based on which a new method for designing high power gain amplifier at frequencies above $f_{max}/2$ is proposed. This method takes into account the variations, modeling errors and losses of the components in the design stage and maximizes the power gain while the stability is guaranteed. The rest of this chapter is organized as follows. A novel stability theory for two-port networks is established in Section 2.2, based on which, in Section 2.3 a design methodology is proposed and a high power gain amplifier is designed in a 130 nm SiGe process. The

measurement results are shown in Section 2.4 which prove the efficacy of the proposed method. Finally, Section 2.5 concludes this work.

2.2 Gain Plane, Stability Region and Normalized Gain Loci

Starting with (1.11) and using (1.10) one can derive [32]:

$$\sqrt{\frac{G_C}{U}} = \left|\frac{A - G_C}{A - 1}\right|. \tag{2.1}$$

This is a fundamental equation relating the three power gains of a two-port network. The advantage of (2.1) over (1.10) is that U and A can be controlled independently. Namely, A can be modified by FPLLR embeddings (which contain feedback) while U is preserved, and if necessary, U can be simply modified while A is kept constant, by adding loss to the input and/or output ports [1, 33]. On the contrary, there is no clear way to modify η and A separately and thence (1.10) cannot be utilized for this purpose.

In the following, (2.1) is studied thoroughly to obtain an intuition and a graphical tool to study power gain and stability of two-port networks.

2.2.1 Gain Plane

A two-dimensional mapping of (2.1) provides us with a very useful graphical tool to study the stability and the power gain of a two-port network. Bearing in mind that A can be varied while U is preserved, (2.1) can be written as:

$$\sqrt{\frac{G_C}{U}} = \left|\frac{1 - \frac{G_C}{U}\frac{U}{A}}{1 - \frac{1}{U}\frac{U}{A}}\right|. \tag{2.2}$$

where the ***normalized gain***, i.e. $k = G_C/U$ is expressed as a function of the complex number U/A. Therefore, a plane (*the gain plane*) with coordinate axes $x = Re(U/A)$

and $y = Im(U/A)$ is exploited to locate the unique loci of constant normalized gain. Moreover, since G_C is defined only when the network is unconditionally stable, it is necessary to determine the stability region in this plane. This stability region along with the constant G_C loci provides a powerful graphical tool to observe the performance of a two-port network as an amplifier. Furthermore, the convex region of stability and the constant gain loci which are derived in the following, are employed in this work within a nonlinear optimization code to design a stable amplifier which provides the maximum possible power gain for all design corners.

2.2.2 Stability Region

A new convex stability region in the gain plane is introduced in this part. In contrary to the well-known $k - \Delta$ stability test [4], this new region shows how close/far the network is to become unstable. As mentioned before, at the boundary of stability $\eta = 1$ and hence $G_C = |A|$. Substituting this into (2.2), defines the boundary of the stability region in the gain plane as follows:

$$x^2 + y^2 = 2(U - U^2)x - U^2 + 2U^4(1 - \sqrt{\frac{U^3 - 2Ux + 2x - U}{U^3}}). \tag{2.3}$$

This stability boundary is shown in Fig. 2.1 along with the locus of $|A| = 1$ which is a circle. It is clear that outside this circle the network is not of any interest since the forward gain is less than the backward gain.

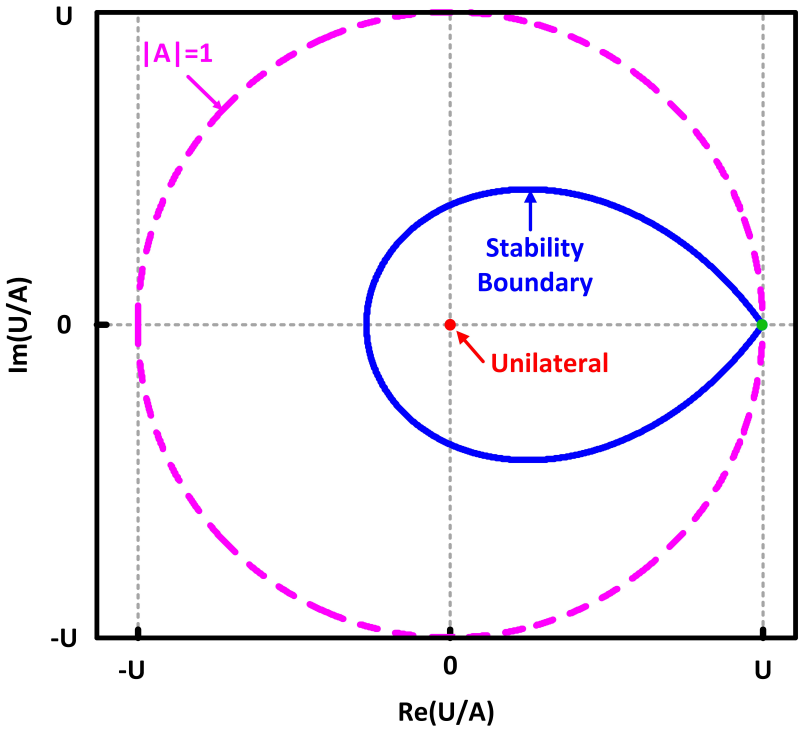

Figure 2.1: The stability region in the gain plane is *inside* the blue boundary (solid). Outside the pink circle (dashed) the device is not useful anymore since $|A| < 1$.

2.2.3 Normalized Gain Loci

Similar to the previous derivation, by substituting $G_C = kU$ in (2.2), it is possible to show that for a fixed *normalized gain* "k", the loci in the gain plane are part of the following circles that lies inside the stability region :

$$(k^2 - \frac{k}{U^2})y^2 + (1 - kx)^2 = k(1 - \frac{x}{U})^2. \tag{2.4}$$

Fig. 2.2 depicts a few of these constant gain circles. The normalized gain is greater than k_0 on the left side of the k_0 constant circle.

A complete set of derived equations of stability boundary, constant gain loci and their intercept points are given in Appendix.

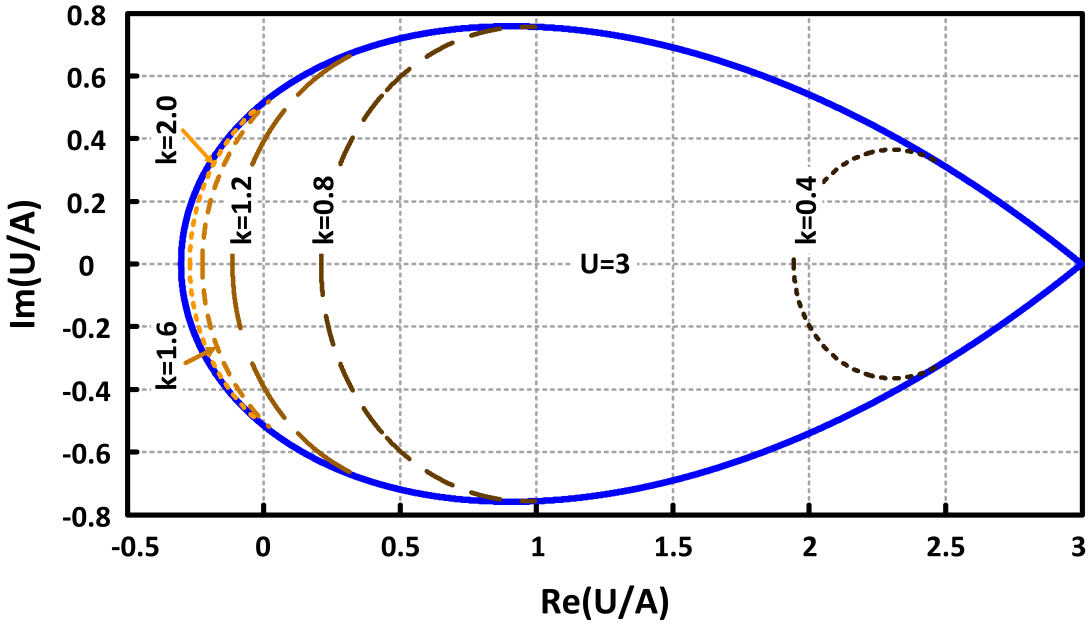

Figure 2.2: Constant normalized gain (k) loci in the *gain plane* depicted for $U = 3$

Having the y-parameters of a two-port network at a desired frequency, we are able to calculate its unilateral power gain (U), its maximum stable gain (A) and thence, the real and imaginary parts of U/A. Therefore, we can map the network into the gain plane and see if it is stable or not and how far from the boundary it is. When it is stable, the given network lies on a constant normalized gain circle of (2.4) where $G_C = k \times U$.

It is worth emphasizing that the existence of the constant normalized gain loci (or similarly the constant G_C loci since $k = G_C/U$ and U is constant under FPLLR embeddings), once more depicts the fact that a two-port network with higher U can provide higher G_C.

Remark 1: The origin of the gain plane corresponds to the *unilateral* network where $G_C = U$ as depicted in Fig. 2.1 (see Appendix). Also, examining the loci of $G_C = 1 \times U$ reveals that there are infinite number of points in the gain plane that result in the same

power gain as unilateralization which do not require to satisfy unilateralization condition ($y_{12} = 0$), i.e. there is no need to cancel the feedback from the output to the input.

Remark 2: $G_{C_{max}} = (\sqrt{U} + \sqrt{(U-1)})^2$ corresponds to the far left intercept point on the boundary of the stability region and the x-axis (see Appendix). This is the maximum possible transducer power gain of a two-port network having unilateral power gain of U, under SCM condition. In case $U \gg 1$, $G_{C_{max}} \simeq 4 \times U$, which is a well-known limit of G_C at low frequencies.

Remark 3: Careful examination of Fig. 2.2, constant gain circles and their interceptions with the stability boundary reveals that in contrary to common belief, being close to instability does not necessarily result in a high gain. To have a high gain we need to be on the left side of the stability region.

This new plane proves more efficient for amplifier design compared to Smith Chart, since it provides loci for constant transducer power gain if SCM, whereas in Smith Chart there is no such concept for G_T.

Remark 4: It is worth mentioning that there are constant gain circles for the available power gain (G_{av}) and also for the operational power gain (G_P) in Smith Chart [4,34] that should not be mixed up with the constant G_C loci in this approach. Those constant gain circles in Smith Chart show the gain variation based on the choice of the load or source impedances and reaching to the center of those circles is equivalent to obtaining a gain equal to the G_C of the given transistor. However, in this proposed method, using an FPLLR embedding the G_C of the transistor is improved by moving towards left side (to the high gain regions) of the stability region in the gain plane. Next, since stability is assured by remaining inside the introduced region of Fig. 2.1, using SCM, the amplifier would come up with a gain equal to this improved G_C.

Remark 5: Although the presented stability region is derived from the equations containing Rollet's factor (K_f), there are two main advantages in this rigorous graphical presentation. First, a convex stability region is introduced which significantly helps, compared to the set defined by $K_f > 1$, to build a well-behaved constraint for a constrained optimization problem which makes it possible to be solved by the existing optimization solvers. In fact, convexifying a problem is a well-known trend in control system theory to make an optimization problem solvable using advanced optimization techniques [35]. The proposed theory provides a convex constraint for the stability of two-port network, whereas the set defined by $K_f > 1$ is a non-convex nonlinear constraint which is strongly misbehaved constraint. Second, the graphical tool in this work makes this theory quite useful for designers to get intuition about the network stability and its sensitivity to changes in different parameters, whereas having $K_f = 10$ or $K_f = 2$, does not provide any insight about how close or far from stability boundary the circuit is and it even does not imply that the former is more stable than the latter. Whereas in the proposed stability plane, the designer can see the movements of the network in the plane caused by the embeddings, parasitics and corners to have a solid understanding about sensitivity of the network with respect to those parameters.

Fig. 2.3 shows how a transistor with emitter length of $2 \times 5\ \mu m$ (and properly biased) in the employed process evolves in the gain plane as the frequency changes from 55 GHz to 180 GHz. As the frequency increases towards f_{max}, the device becomes stable and U decreases which results in a smaller stability region as depicted in Fig. 2.3.

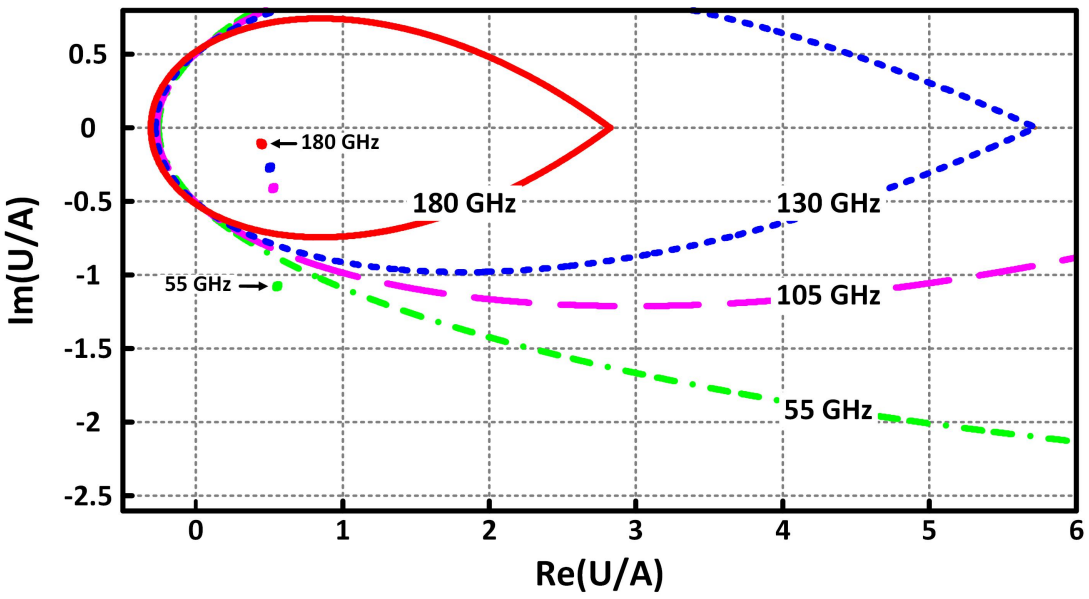

Figure 2.3: As frequency increases from 55 GHz to 180 GHz, stability region shrinks and the transistor moves inside stability region.

2.3 High Power Gain Amplifier Design

In this part, a new method to design a high power gain amplifier is suggested. By providing enough degrees of freedom for an FPLLR embedding similar to Fig. 2.4, it is possible to move a two-port active network over the gain plane towards the left to improve k while U is constant.

In order to design a high power gain amplifier, first of all, the transistors and their bias points should be selected.

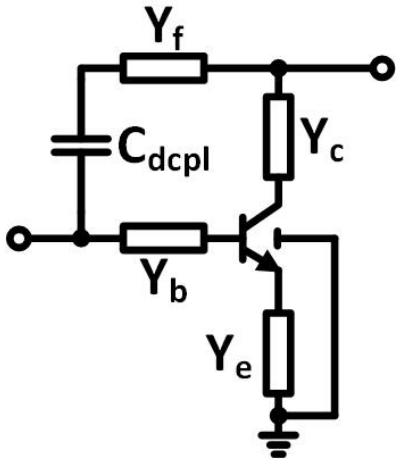

Figure 2.4: Proposed FPLLR embedding which provides enough degree of freedom to move the circuit towards high gain region

2.3.1 Transistor and Bias Selection

Since the power gain of an amplifier is closely related to its unilateral power gain, the device size and bias should be selected such that its U is maximized. Usually, as the device size (the emitter length of a bipolar transistor in this case) increases, its maximum U decreases (see Fig. 2.5). Meanwhile, as the size increases, the maximum U of the transistor happens at higher bias currents (see Fig. 2.6) and becomes more flat, i.e. its sensitivity with respect to the bias current decreases (see Fig. 2.7).

The noise of a transistor and its output power are closely related to its bias current and the power budget of the circuit. Similar to power amplifiers, the output power is a portion of dc power. Therefore, based on the desired output power and/or noise performance of the amplifier, the bias current is selected and then the transistor size can be found from Fig. 2.6 such that the transistor be in its most active (optimum) condition.

For the sake of completeness, the evolution of a transistor in the gain plane with

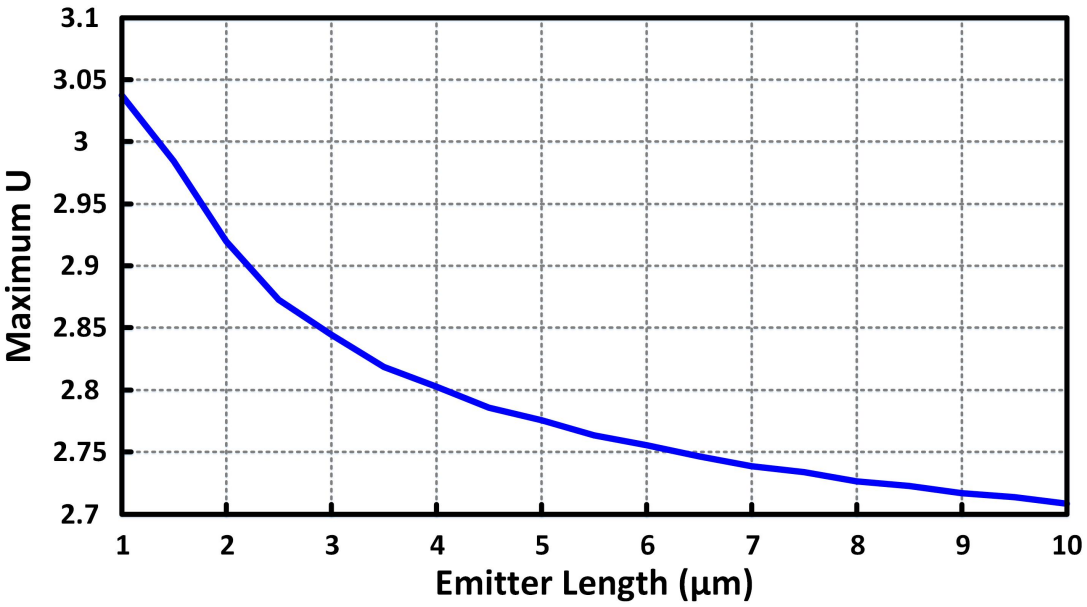

Figure 2.5: Maximum U at 180 GHz for different total emitter lengths (one finger) in a 130 nm process

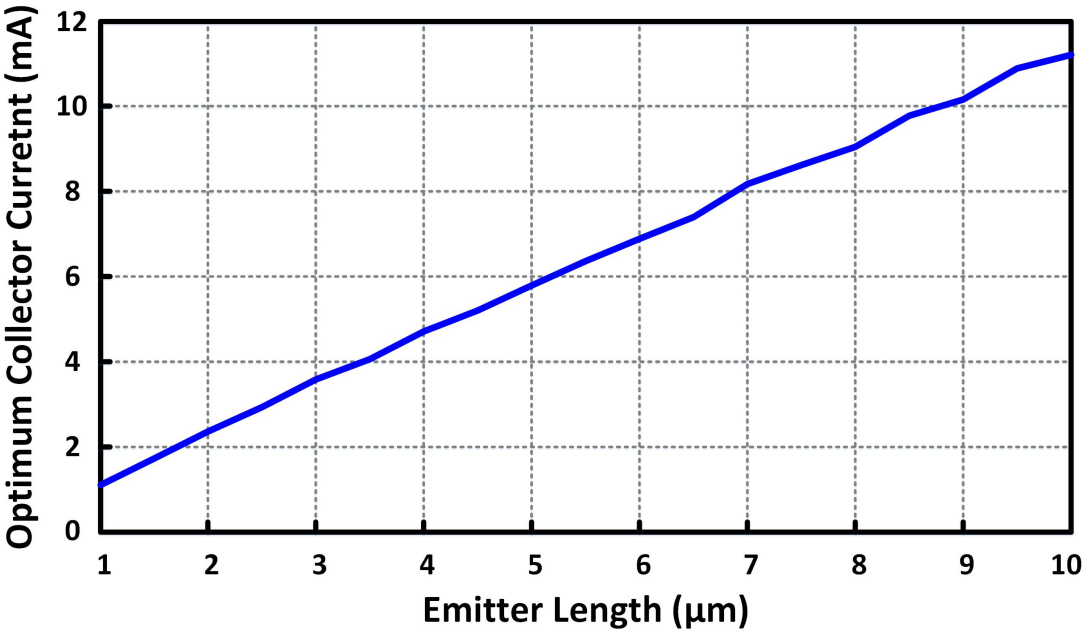

Figure 2.6: Collector current at which U becomes maximum for different total emitter lengths (one finger) at 180 GHz in a 130 nm process

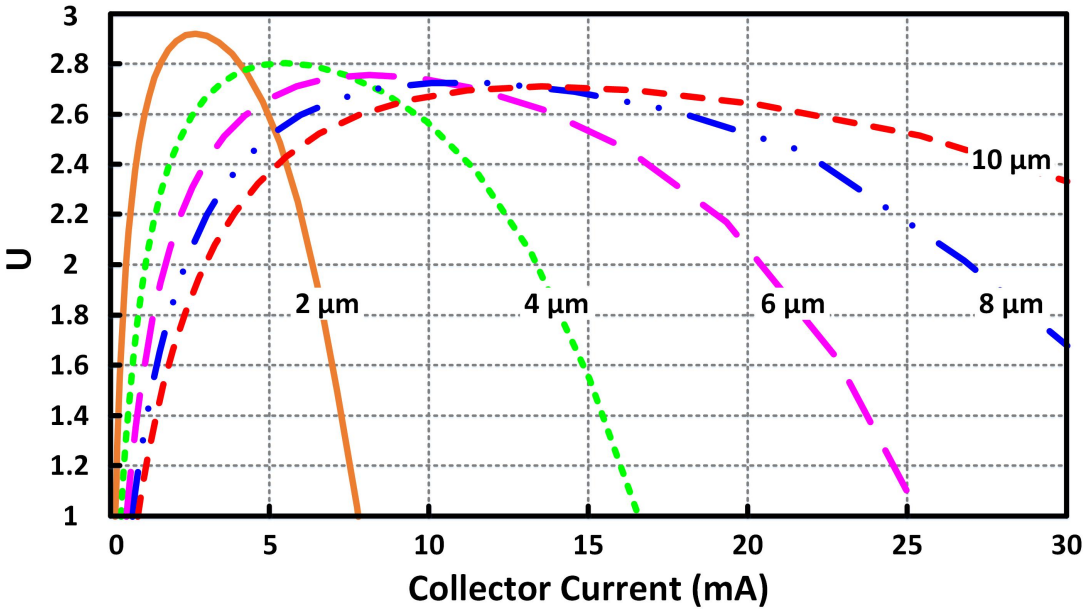

Figure 2.7: U vs. I_c for different total emitter lengths (one finger) at 180 GHz in a 130 nm process

bias current is shown in Fig. 2.8. For a selected emitter length (selected size from Fig. 2.6), changing the number of emitter fingers, slightly changes the parasitics of the transistor and hence affects the U moderately. Depending on the desired frequency and the selected structure for the embedding, larger C_μ might help/hurt the feedback which is supposed to partially resonate C_μ out. In this work, based on all these considerations and trade-offs, the transistor is chosen to have a total emitter length of 4.2 μm. After choosing the total emitter length, the number of fingers is chosen such that the highest U is achieved. This results in selecting a transistor with 3×1.4 μm emitter length. Figure 2.9 shows G_C and G_{msg} of this device at the selected bias current. As mentioned in the abstract, a three stage amplifier employing this device results in 6.8 dB power gain at 180 GHz assuming perfect conjugate match (see Fig. 2.9).

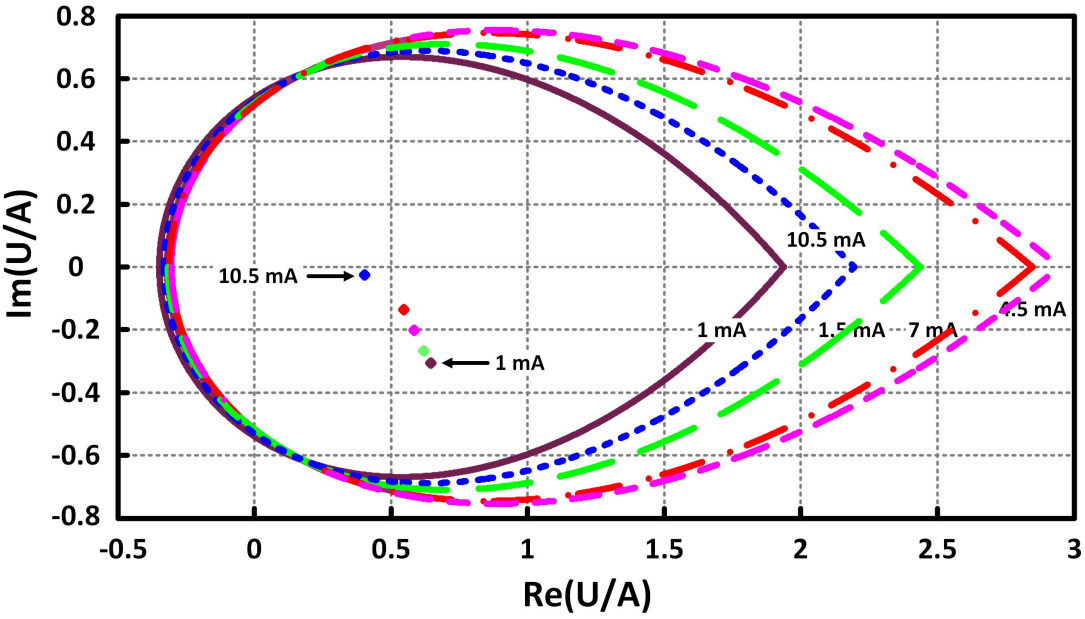

Figure 2.8: Evolution of a transistor with emitter length of $3 \times 1.4\ \mu m$ as bias current increases from 1 mA to 10 mA at 180 GHz in a 130 nm process

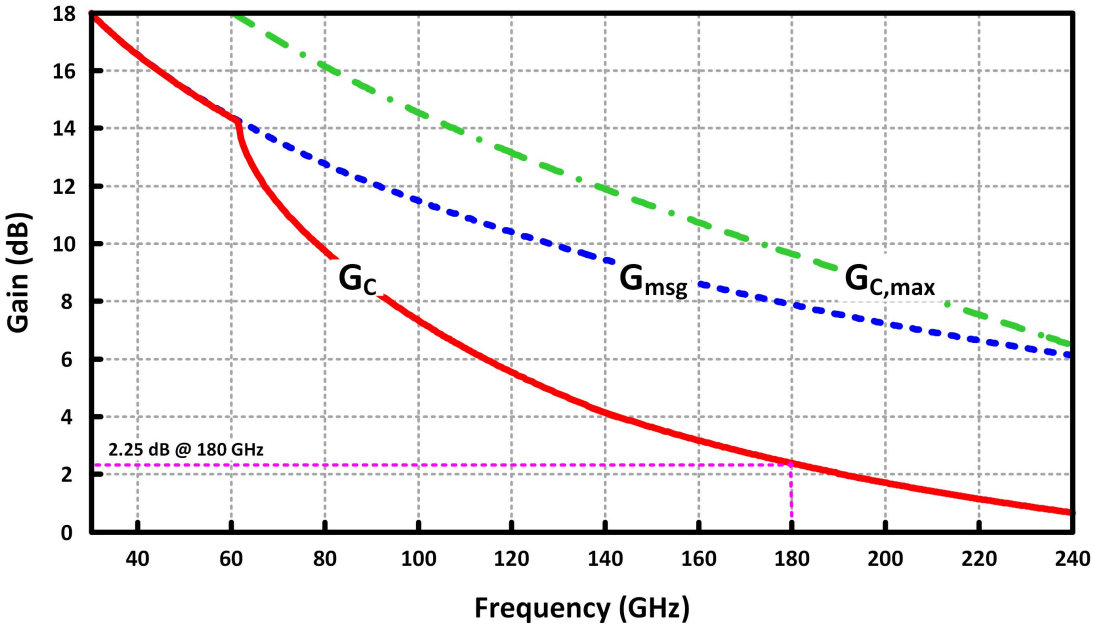

Figure 2.9: G_C, G_{msg} and $G_{C,max}$ of the selected $3 \times 1.4\ \mu m$ transistor biased at optimum collector current in a 130 nm process vs. frequency

2.3.2 Passive Components Considerations

As the next step, the structure of the passive components should be defined. Primary optimization using ideal components for the embedding circuit shows that in order to be able to move the employed transistor to the left of the gain plane, Y_b, Y_c and Y_f have to be inductive and Y_e needs to be capacitive. This result is transistors/processes dependent and has to be found either by intuition or by optimization using ideal components.

Remark : It is worth mentioning that since Y_f and Y_b are distributed components, they are not interchangeable in Fig. 2.4, and because of this, this structure provides adequate degrees of freedom for the embedding.

Transmission Lines

The transmission lines Y_c, Y_f and Y_b are realized as grounded coplanar wave guides (GCPW). This structure provides decent shielding at high frequencies [36] as well as a low-loss return path. The patterned ground plane of the GCPW's is composed of stacked three lower metal layers to provide adequate thickness for reducing the loss (while not being too close to the signal track). It is patterned to decrease the formation of Eddy current loops so that the inductance and thence the characteristic impedance of the line (Z_0) be preserved in the presence of the ground plane. In order to have high quality (low loss) transmission lines, α/Z_0 of the line should be minimized [36] (α is the real part of the propagation constant ($\gamma = \alpha + j\beta$)). This can be studied in HFSS using Optimetrics tool. Intuitively, assume that the distance between the walls is larger than the distance between the signal track and the ground plane. This is a reasonable assumption since the distance in the latter is usually less than a couple of micrometers. Hence, due to proximity of the ground plane and also the skin effect, most

of the current flows on the bottom surface and less on the side walls of the signal track. Therefore, further increasing the distance of the walls from the signal track does not affect the current distribution significantly and thence the loss (α). However, increasing the distance between the walls improves the Z_0 at first and soon saturates and is not worth the area after a certain distance. Thus, the distance between the walls is usually selected based on the area availability. On the contrary, the width of the signal track significantly affects both Z_0 and α. The narrower the track width, the larger both Z_0 and α. Thus, for a given wall distance there is a track width at which α/Z_0 becomes minimum for the desired operation frequency. The thickness of the walls can simply be chosen a couple of micrometers since this way it would be much thicker than the ground plane and usually much farther than that and hence accommodates less return current. Therefore, its conductance has a minor effect on the quality factor of the transmission line. Here,for the operation frequency of 180 GHz, the walls are chosen to be 5 μm thick, the width of the signal track is 3 μm and the inner distance between the walls is 40 μm.

Capacitor at Emitter

Y_e is a capacitor with one node connected to the emitter and the other one grounded. Therefore, we need a choke (a quarter wave length transmission line) for bias current. To decrease the energy loss by radiation and also to avoid signal coupling to the substrate and to the rest of the circuit, one plate of C_e is realized as a box in first and third metal layers (connected in three edges, using vias) and the other plate which goes in between, is on the second metal layer connected to the emitter. Since the connecting track is very short, the resonance frequency of this capacitor is very high and hence its quality factor is very high even though it is fabricated in lower thin metal layers. The choke is realized

as a quarter wavelength GCPW transmission line. According to the EM simulations, the quality factor of the combination of the choke and the capacitor is around 20 at the desired frequency. This grounded capacitor which is made using first three metal layers along with the choke can be simply modeled by an ideal capacitor in parallel to a resistor.

Decoupling Capacitor

The decoupling capacitor (C_{dcpl}) is not part of the optimized circuit, because primarily it is used to decouple the dc voltages of collector and base and ideally it has to be large enough in order not to affect the impedance of the inductive feedback. However, to have a reasonable size and avoid poor quality factor and large parasitics to the ground (which degrade U), it cannot be very large. Moreover, there is another advantage not to have a very large C_{dcpl} that is not short circuit at the desired frequency. In this case, the transmission lines Y_f and Y_b need to be longer to be able to resonate out this capacitor. This makes these two transmission lines more practical for fabrication at this frequency range. The longer the transmission lines, the lower the proportional variations and modeling errors. Here, C_{dcpl} is designed as a finger capacitor in two top metal layers.

All passives are modeled using HFSS and hence their models include all losses and non-idealities. The final structure has to be EM simulated as a whole to verify that the resultant network has the same expected mapping into the gain plane.

2.3.3 Optimization

Having the *y*-parameters of the network, the optimum value of the embeddings should be found. Using parametric analysis tool in Cadence it is possible to find an embedding which shifts the network close to the point of G_{Cmax} (the farthest left point on the stability boundary) to get the highest possible gain from the employed transistor. However, the resultant circuit is usually so sensitive to the variations and modeling errors of each component such that a very small deviation from the desired values results in a huge shift in the gain plane, which leads to either instability or low power gain. This indicates that finding an FPLLR embedding to move the network to the high gain stable regions is a very unreliable design method using Cadence parametric analysis tool. Even forgetting about the sensitivity, which is not an option, finding an embedding with four independent components in a reasonable range, requires a huge number of steps which makes it almost impossible to be done in any circuit design tool such as Cadence and ADS.

In fact, we need a method which is capable of finding the embedding while it considers the variations and modeling errors *"during the design process"*, to guarantee that even if the worst case happens, the network remains stable and provides a decent power gain. That is, the corners must not be considered after the design is done merely to perform an analysis to see how they affect the performance of the circuit. We need to take into account all corners in the design stage to make sure that all of them will perform.

In general, a constrained optimization solver can optimize the power gain, while the desired constraints are satisfied. It provides the possibility to maximize the minimum power gain of all considered corners while all of them remain inside the stability region. Similar to the corner analysis, we can assume a typical, a min and a max model for each component to find the circuit corners. For instance, assume that the embedding is composed of one capacitor (with two corners and one typical model) and a transistor which

has typical, bmin and bmax corners. In this case we can think of nine different corners for the whole network. However, usually the extreme cases cover all possibilities such that we need to consider only four corners composed of the combination of the extreme cases of transistor and capacitor. We always take into account the typical case as a reference, and hence we will have four corners and one nominal circuit for this example. Next, we need to find the capacitor such that the power gain of the corner with minimum gain (which is unknown in each iteration before calculating the gain of all corners) is maximized, while all five circuits remain stable. We can also add a margin not to let any of the corners get very close to the stability boundary. However, it is not necessary since all reasonable variations and modeling errors are already included in the corners and we do not expect more change in the fabricated circuit if the considered corners are adequately reasonable. In general if there are n components with foreseeable errors and variations within a reasonable range, there would be 2^n corners and one typical network that all must remain stable while the embedding is chosen such that the gain of the corner with minimum gain is maximized.

The mentioned optimization problem is a constrained polytopic problem [37, 38] maximizing the minimum power gain among all considered corners over the convex stability set.

Given the decoupling capacitor and the biased transistor, the high gain amplifier design can be formulated as follows:

$$\max_{\boldsymbol{Y_f},\boldsymbol{Y_b},\boldsymbol{Y_c},\boldsymbol{Y_e}} \{\min_{i} \boldsymbol{k_i}\}$$
$$\textbf{such that:} \tag{2.5}$$
$$\tfrac{U_i}{A_i} \in \text{Convex Stability Region in (2.3)}$$
$$i = 1, \ldots, 17,$$

where

$$k_i = \frac{G_{Ci}}{U_i}.$$

Such a problem can be solved using an appropriate constrained optimization solver. Implementing the above problem in a code is simple but the problem itself is quite nonlinear and the original functions of MATLAB such as `fmincon` cannot solve it easily and efficiently. Efficient practical techniques [39] are exploited to simplify the problem for the solvers. A MATLAB code is developed which employs Sparse Nonlinear Optimizer (SNOPT) [40] in order to find the best embedding composed of the transmission lines and capacitors which are modeled using HFSS. A complete table of the y-parameters of each passive components in a reasonable range of values should be provided to the code so that it can find the optimum embedding. It is simple to use a regression method to find the intermediate values if the steps are adequately fine. For instance, considering the fabrication accuracy, it is sufficient to provide the y-parameters of the transmission lines in steps of 5 μm up to half the wave length at the desired frequency.

The results show that instead of shifting the whole circuit towards the far left point on the real axis inside the stability region (i.e. towards G_{Cmax}), the solver has pushed all corners to another spot close to the left side of the region in order to accommodate all corners inside the stability region. As depicted in Fig. 2.10 the corners might be far from each other in the gain plane. This means we would fail to find the embedding by moving

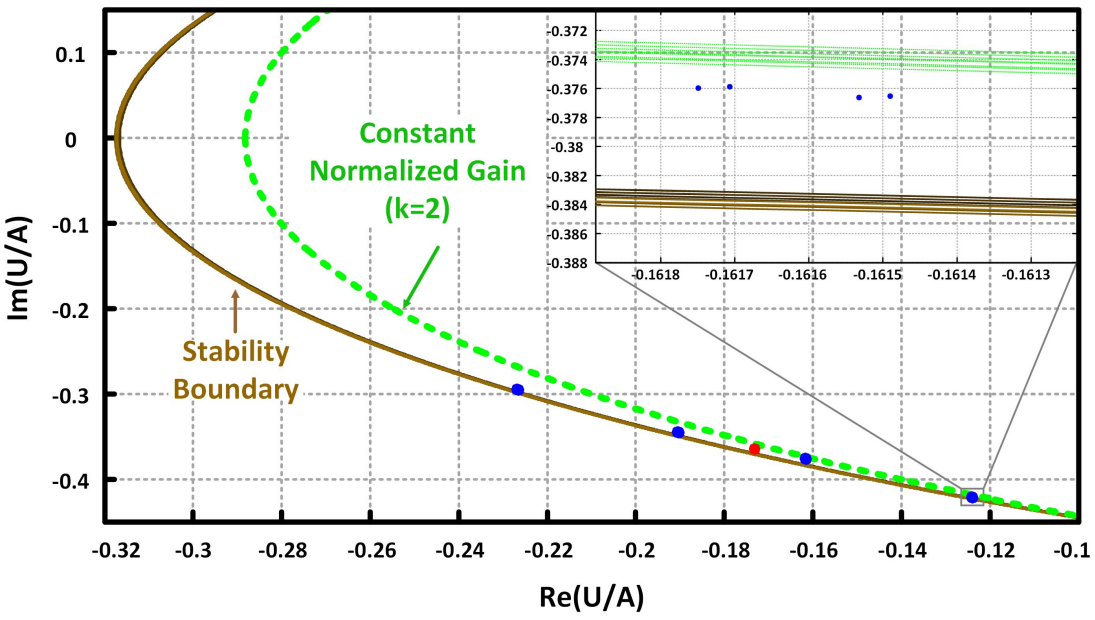

Figure 2.10: Optimized Design where all corners are stable and the minimum normalized gain is more than 2. *Red*: nominal circuit, *Blue*: 16 corners, *Solid Brown:* 16 stability boundaries for different corners (which are slightly different since U is different for each corner because of different losses), *Dashed Green:* loci of normalized gain $k = 2$ for all corners; any point on the left side of these green circles and inside the stability region has a power gain larger than $2 \times U$.

the nominal circuit towards the high normalized power gain regions without knowing the sensitivity of the circuit with respect to each component and how the corners might move in the gain plane away from the nominal network. This complicated problem is efficiently solved by SNOPT.

Remark 1: The advantage of using the proposed stability region in the optimization problem instead of the traditional stability factors such as $k_f - \Delta$ is that it forms a convex constraint which helps the solver to handle the problem very efficiently. Besides, as already mentioned, mapping the network into the gain plane, provides a good understanding about how close to instability we are, and also how close to the maximum theoretical gain the network is. Furthermore, it is a intuitive and graphical way of

understanding gain and stability of a two-port network.

Remark 2: Figure 2.10 clearly shows that if the stability boundary for large U which intercepts x-axis at -0.25 was used for the design, then the gain would definitely be lower than $2 \times U$ since the gain loci with $k = 2$ intercepts x-axis at -0.29.

2.3.4 Input, Output and Interstage Matching

Matching networks are necessary at the input, output and between the stages in order to enhance the power flow and avoid power reflection and loss. There are two main issues regarding the matching circuits at high frequencies.

First, the coupling between the structures becomes very important at high frequency and might degrade the matching performance severely if it is designed separately. Therefore, matching networks have to be EM simulated with the rest of the circuit which makes its design difficult and time consuming.

Secondly, because of the considerable loss in the matching network, particularly due to skin effect at high frequencies, bilateral conjugate-matching is theoretically impossible. Namely, in Fig. 2.11, if $Z_s = Z_{in}^*$ and the matching network is lossless, then Z'_{in} would be equal to 50Ω. However, because of the loss in the matching network, $Z_s = Z_{in}^*$ does not imply $Z'_{in} = 50\Omega$. Hence, it is possible to choose either to have $Z'_{in} = 50\Omega$ or $Z_s = Z_{in}^*$ or we have to find something in between. Therefore, designing a matching network is a challenging problem at high frequencies and in particular, interstage matching is more difficult and if not handled delicately, it can degrade the performance of the circuit drastically.

Here, all matching networks are composed of a piece of GCPW transmission line

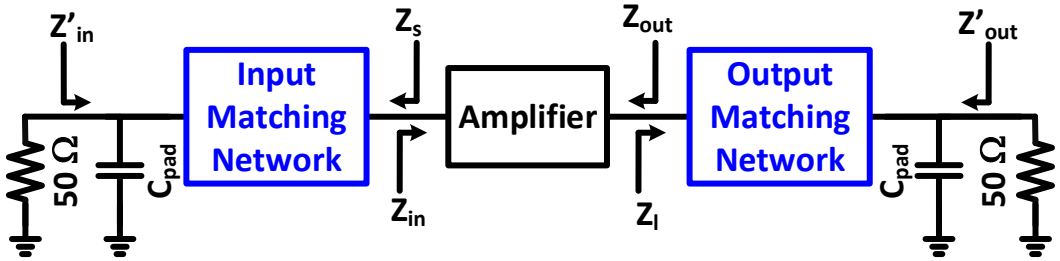

Figure 2.11: Lossy matching network provides unilateral conjugate matching instead of bilateral conjugate matching that a lossless matching network provides. Namely, either $Z_s = Z_{in}^*$ or $Z'_{in} = 50\Omega$.

and possibly a capacitor at each end. Capacitors must be connected to the top metal (to the signal track) and hence there are a set of lossy and inductive vias that connect them together. The distance of the top metal to the bottom metal in the employed process is around 10 μm which is long enough to degrade the quality factor of the employed capacitors at 180 GHz by decreasing its self-resonance frequency and by its loss. Figure 2.12 demonstrates the input/output and interstage matching traces on the Smith chart for performing complex conjugate matching.

2.3.5 Design Example: A Three-Stage Amplifier

Based on the above proposed method, an three-stage amplifier is designed in this part. At first a one-stage amplifier is designed. Using interstage matching networks, a three-stage amplifier is built upon this one-stage optimized amplifier. As already mentioned, the circuit of Fig. 2.4 is employed to provide enough degrees of freedom for the embedding to be able to move the network to the desired region of the stability set in the gain plane.

In order to have a robust design, all worst case scenarios must be taken into account.

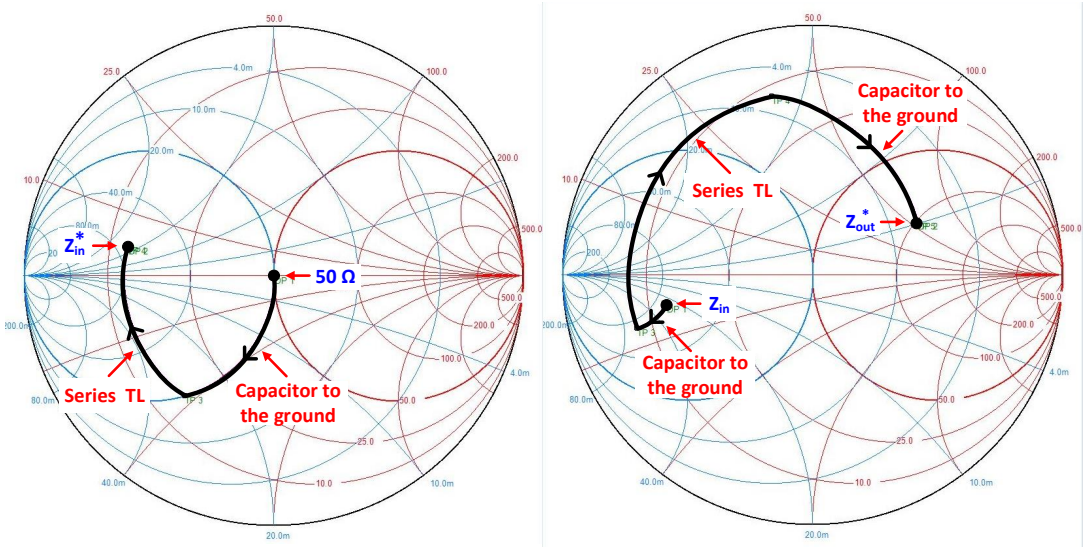

Figure 2.12: Input and interstage matching traces on Smith chart for conjugate matching. The output matching trace is similar to that of input, both start from 50 Ω and move toward the complex conjugate of the input/output impedance.

We assumed that the passive components if large, bear ±5% variation and if small (e.g. Y_b and Y_c usually) bear up to ±15% of error and/or variation. These errors are considered to cover any possible deviation from the typical design, inter-die and intra-die, temperature variations, modeling errors and etc.

In order to attain a reasonable power gain considering all losses, variations and modeling errors, it is preferred not to go beyond $\frac{2}{3}f_{max}$ where U is approximately $(3/2)^2 \simeq 3.5$ dB and the $G_{C,max} \simeq 8.3$ dB. The f_{max} of the employed 130 nm BiCMOS process is ~280 GHz [41]. Therefore, we design an amplifier around $\frac{2}{3}f_{max} \simeq 180$ GHz in order to achieve a reasonable gain.

Providing the y-parameters of each component and the selected transistor at its desired bias point the optimization problem is solved which finds the length of the transmission lines and the capacitance of C_e. To simplify the problem and decrease the num-

Table 2.1: Optimization results

Component	**Value**
Y_b: Transmission line	Length = 24.1724 μ m
Y_c: Transmission line	Length = 5 μ m
Y_f: Transmission line	Length = 196.649 μ m
Y_e: Capacitor	Capacitance = 28.7537 fF

ber of variables, the variation/error of the transistor, Y_e and Y_c are combined all together and Y_f, Y_b and C_{dcpl} each has separate corners. This way, there exists 16 corners which are the worst cases and also one nominal/typical network. Among all these networks, the code maximizes the minimum normalized gain while constrained by the stability of all 17 corners. For the selected transistor, bias and frequency, the solver has come up with the values shown in Table 2.1, which results in the worst case normalized gain of $k = 2.03197$.

The mapping of the nominal circuit and also those of 16 corners are shown in Fig. 2.13. For each corner, U is slightly different (because of different losses) and so are the stability regions and the constant gain loci.

The complete schematic of the three stage amplifier is shown in Fig. 2.14 along with its die photo which is fabricated in 130 nm SiGe process. The whole passive structure including stacked vias to the base, emitter and collector, the transmission lines, capacitors and also dc and signal pads are carefully Em simulated using HFSS, in order to capture the layout parasitics and all the couplings. The simulated G_T, G_{msg} and $G_{C,max}$ of the designed three stage amplifier are shown in Fig. 2.15. It is worth mentioning that by considering errors and variations in each component in the design level, i.e. during the optimization, the imperfections in the layout such as a bending GCPW whose model

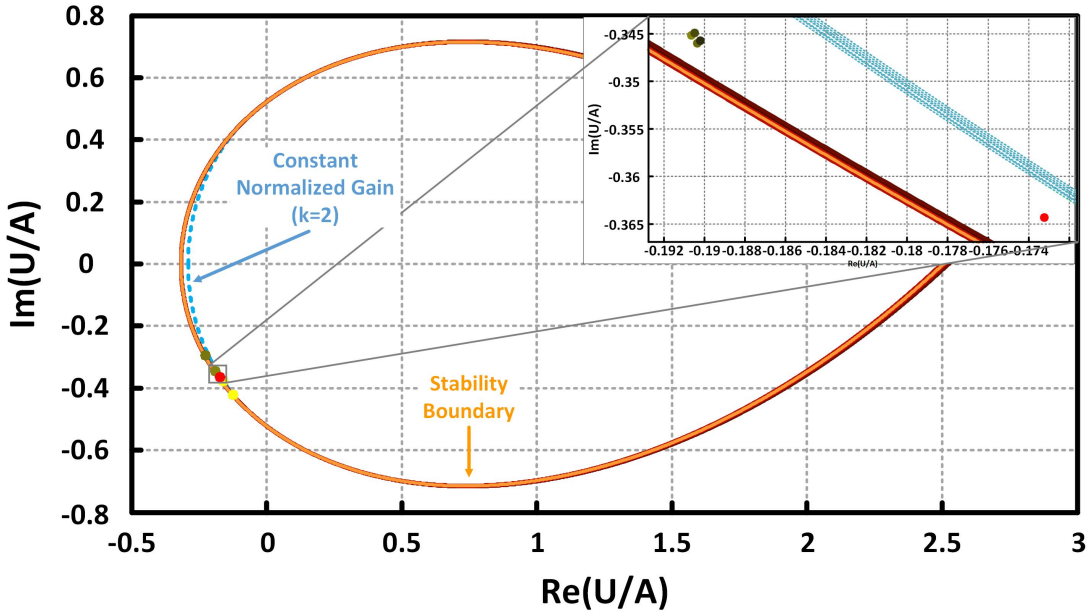

Figure 2.13: Solid lines: Stability boundaries for all corners and nominal circuit, Dashed lines: Loci of normalized power gain $k = 2$ for all corners and nominal circuit. Dots: The nominal circuit and 16 corners on the gain plane

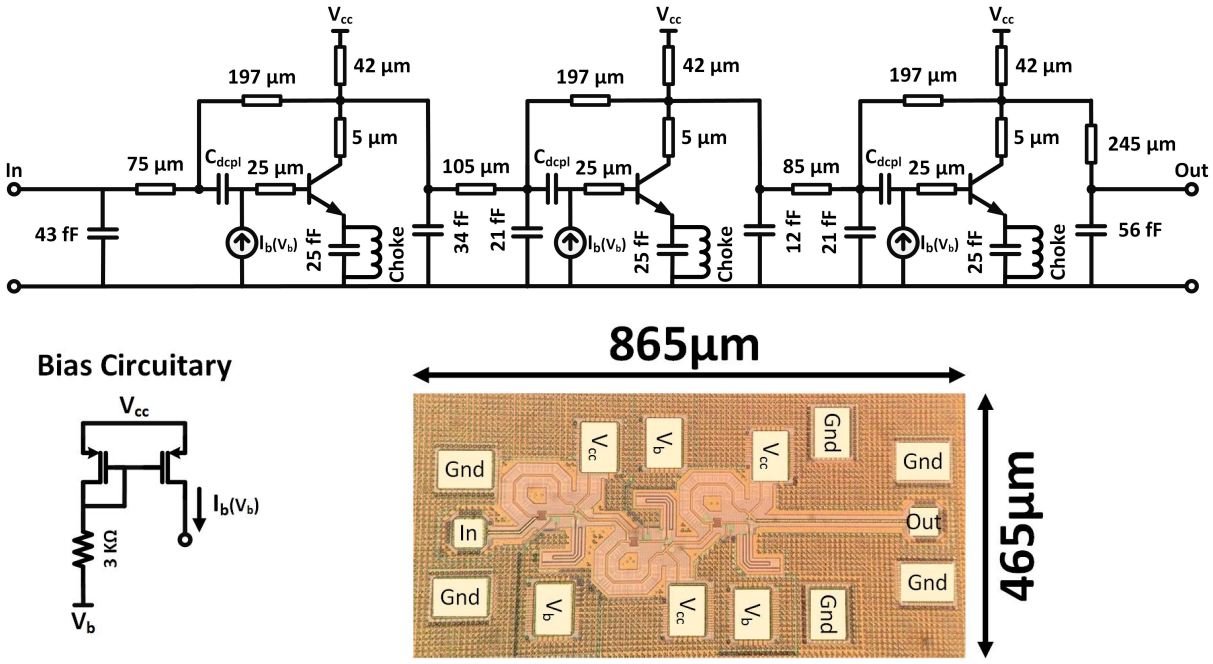

Figure 2.14: Three-stage amplifier schematic and die photo

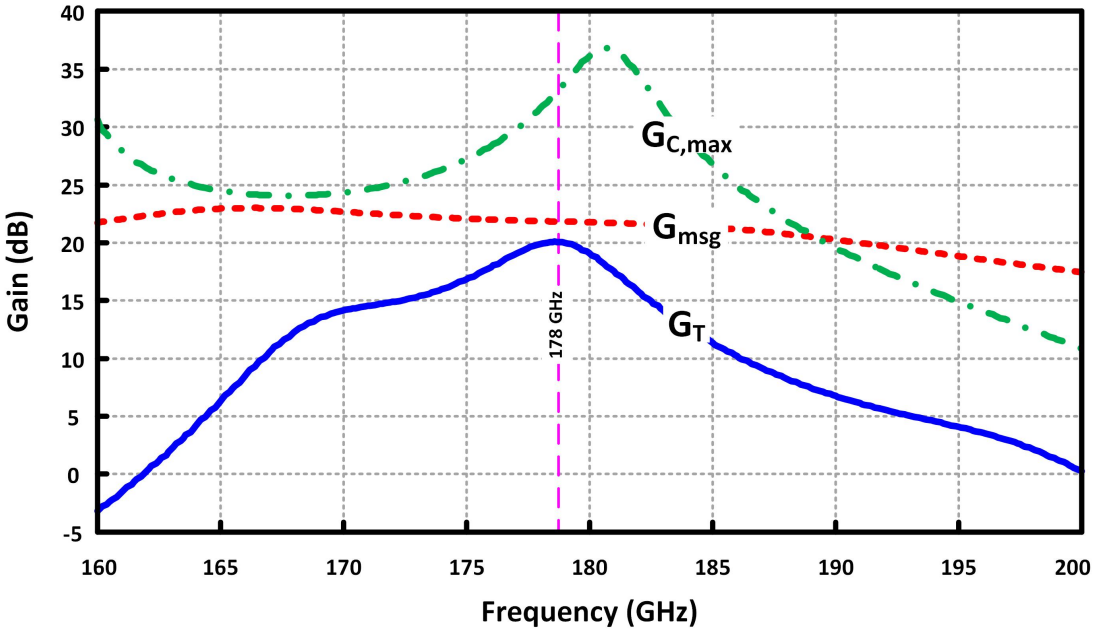

Figure 2.15: simulated G_T, G_{msg} and $G_{C,max}$ of the three stage amplifier in a 130 nm process

slightly deviates from the straight one, would not affect the performance of the resulting amplifier significantly.

2.4 Measurement Results

The employed setup for measuring the S-parameters is depicted in Fig. 2.16. A 67 GHz PNA-X is used along with VDI WR5.1 extenders which are connected to two Cascade I-220 GSG probes via WR5.1 S-bends. The whole measurement setup is calibrated up to the probe heads with minimum possible input power level in order to measure the small signal S-parameters.

The measured S-parameters are shown in Fig. 2.17 along with the simulation results.

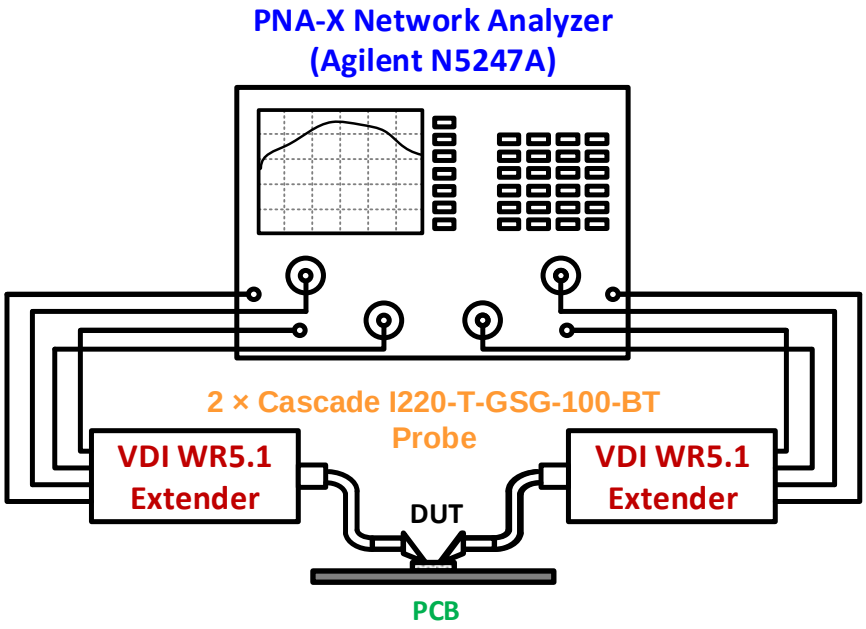

Figure 2.16: S-parameters measurement setup

The measured results show a reasonable 8.2 GHz 3 dB band width and a power gain of 18.5 dB at 173 GHz while consuming 42 mW dc power from 1.8 V supply. The measured stability factor is shown in Fig. 2.18 which indicates that the amplifier is stable.

Figure 2.19 demonstrates the setup which has been used to measure the large signal behavior of the amplifier. The input power is swept using PNA while the output power is measured using VDI Erickson PM4 power meter. The saturated output power is 0.9 dBm. The results are shown in Fig. 2.20.

Table 2.2 compares the results of the state of the art methods and that of this work. As already mentioned, the maximum power gain that a device can provide is directly related to its unilateral power gain independent of the frequency or the employed process. Hence, to be able to compare different methods independent of the employed processes,

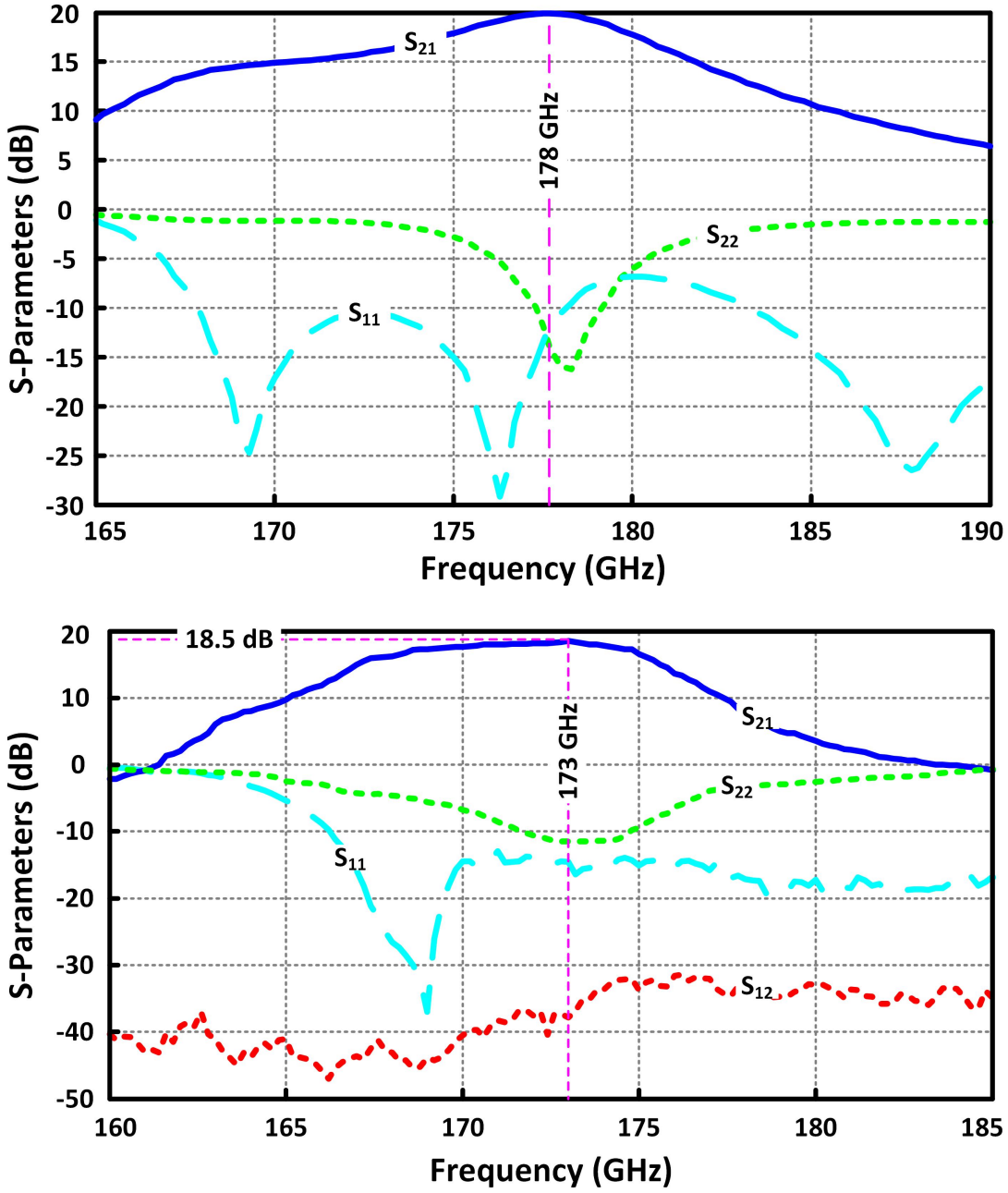

Figure 2.17: The S-parameters of the designed three stage amplifier, Top: simulated, Bottom: measured

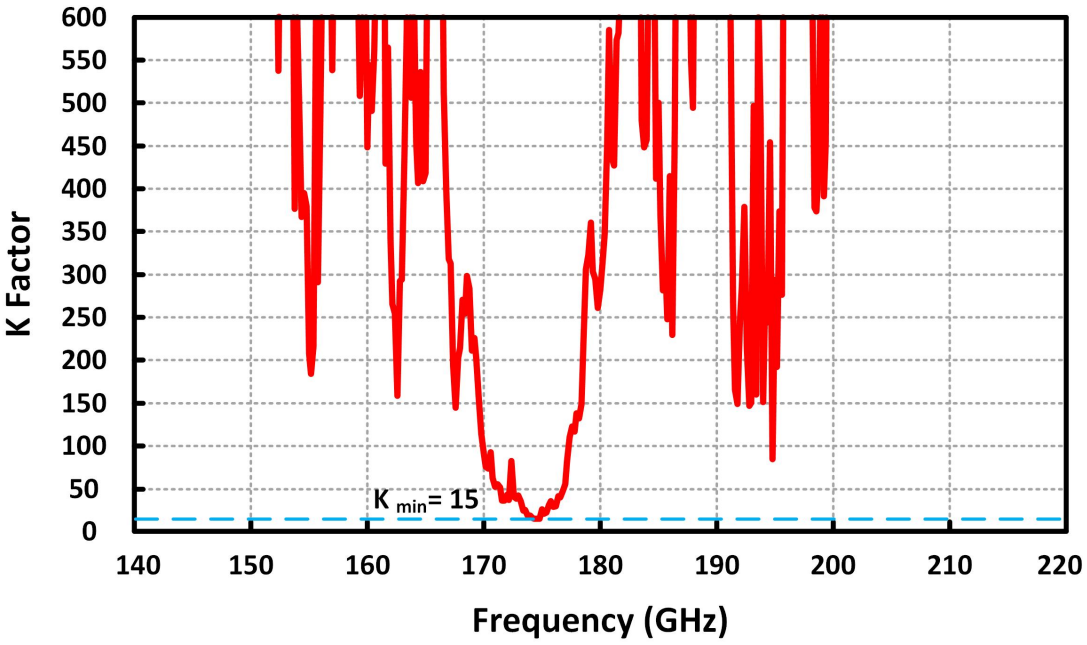

Figure 2.18: The measured stability factor of the amplifier

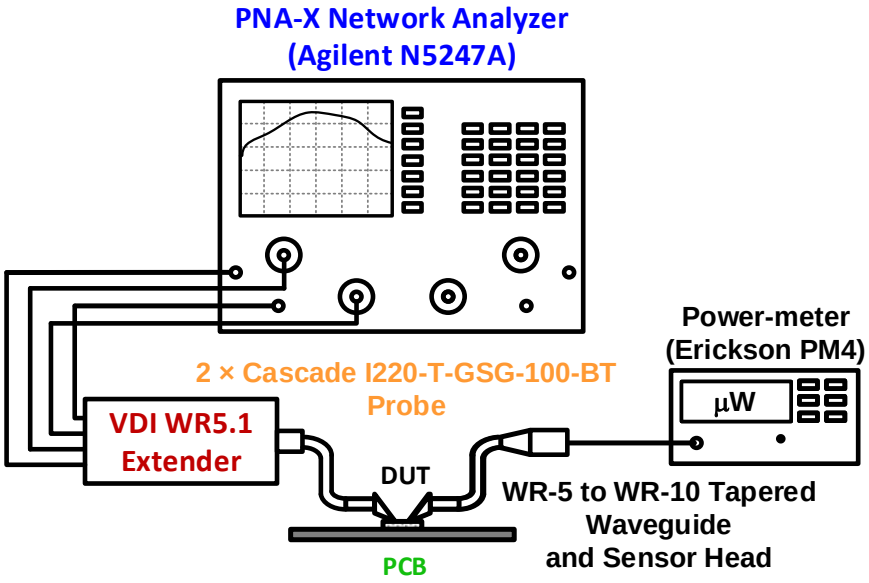

Figure 2.19: Large signal measurement setup

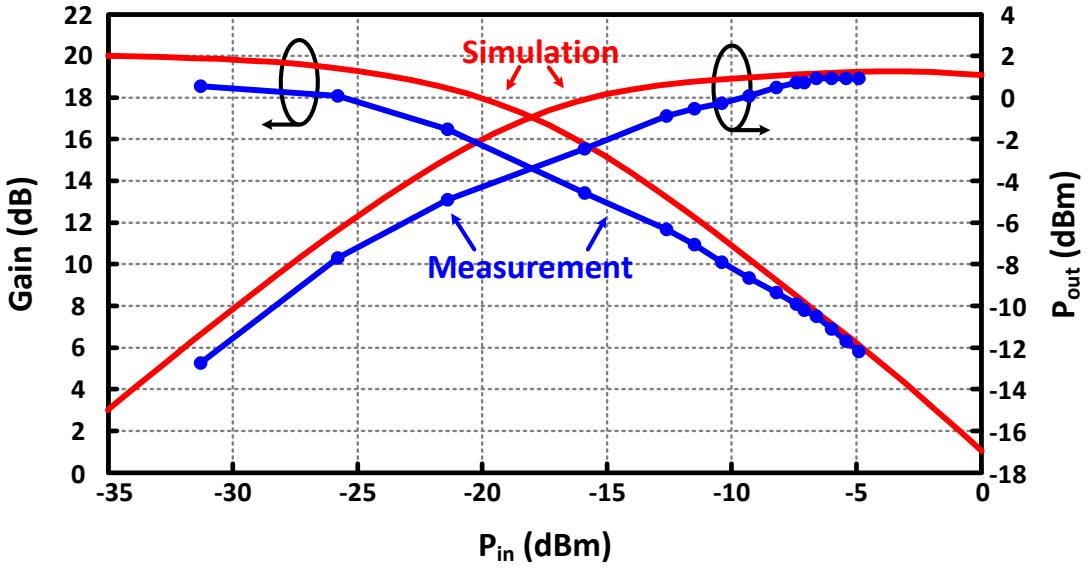

Figure 2.20: Large signal measurement of the output power and gain versus input power

the normalized power gain of each stage of the resulting amplifiers must be compared. The FoM is defined as :

$$FoM = \frac{\sqrt[n]{G_T}}{U(f)}, \tag{2.6}$$

in which n is the number of gain devices and $U(f)$ is the unilateral power gain of the employed device at the operation frequency. This FoM shows how efficient a design procedure extracts the maximum possible gain out of each active device. As shown in Table 2.2, the results of this work clearly prove the effectiveness of the proposed method.

Remark: It is noteworthy that dc power consumption is not directly included in the FoM. As discussed before, maximum power gain of a device is solely related to U (and thence to the f_{max} of the process). On the other hand, transistors of different processes achieve their maximum U (at the desired frequency) in different bias currents (and different current densities), i.e. similar dc power consumptions do not result in similar U in different processes. To clarify this point,consider two unilateralized single-stage ampli-

fiers designed in two different processes using ideal passives, both at a frequency where $U = 4$. These two amplifiers will have identical power gain of 4. Since the method is exactly the same and passives are ideal, the FoM should be similar. However, usually these two amplifiers consume different dc powers to result in a power gain equal to the U which means same unilateralization method does not achieve the same FoM in two different processes if dc power consumption is included in the FoM. In other words, dc power would be different while the method and its ability to extract power gain out of the device is the same, i.e. $G_C/U = 1$ in both cases. This example clarifies that including dc power in the FoM leads to misleading results when considering the efficacy of the method in extracting power gain from the device. In fact, it is not fair to compare two design methods in two different process while one of the process specs (dc power consumption) is playing an important role in determining the FoM. The proposed FoM is defined to fairly compare different amplifier design methods independent of the process and solely by comparing the efficiency of the utilized method in achieving high power gain.

2.5 Conclusion

A novel systematic approach to design high gain amplifiers above $f_{max}/2$ of the utilized transistor is proposed. In order to find the best embedding that can extract the maximum possible gain out of the active device, a new stability theory is developed. An optimization solver finds the embedding to maximize the power gain while all considered corners remain inside the developed convex stability region. The resulting three-stage amplifier has the best normalized power gain compared to all previous designs considering the capability of the utilized transistors at the operation frequency.

Table 2.2: Comparison Table

	Freq. (GHz)	**Gain** (dB)	P_{sat} (dBm)	P_{dc} (mW)	f_{max} (GHz)	$U(f)$ (dB)	**3 dB BW** (GHz)	**FoM**
[22]	140	8	-1.8	63	240	4.7	10	0.46
[23]	140	18	NA	112	300	6.63	18	0.5
[24]	144	20.6	5.7	54.6	240	4.42	-	0.8
[42]	150	8.2	6.3	25.5	320	6.6	27	0.41
[43]	170	15	> 0	135	340	6	10	0.39
[44]	200	17	> -3.5	18	450	7	44	0.53
[45]	210	15	NA	144	435	6.33	30	0.41
[46]	213	10.5	-3.2	42.3	275	2.21	13	0.79
[30]	233	22.5	NA	68	450	5.72	10	0.51
[31]	257	9.2	-3.9	27.6	350	2.68	12.2	0.86
This work	**173**	**18.5**	**0.9**	**42**	**280**	**4**	**8.2**	**1.65**

2.6 Appendix

In order to be able to define the stability constraints and optimizing the power gain, we had to derive many related equations. Here we provide some of those equations we have derived for the first time. The stability region has a boundary composed of two parabolas:

$$y^2 + x^2 = 2Ux - 2U^2\sqrt{\frac{U^3 - 2Ux + 2x - U}{U^3}} - 2U^2x - U^2 + 2U^4 \tag{2.7}$$

where $x = Re(U/A)$ and $y = Im(U/A)$. The closed convex stability region intercepts x-axis at $x = U$ and

$$x = U + 2\sqrt{U^4 - U^3} - 2U^2 \leq -0.25.$$

It intercepts vertical axis at

$$y = \pm\sqrt{2U^3\sqrt{U^2-1} - U^2 + 2U^4}$$

which approaches to ±0.5 as $U \to \infty$. As $U \to \infty$, the stability region becomes:

$$y^2 \leq x + 0.25, \tag{2.8}$$

which is a parabola open towards the positive horizontal axis and intercepts the x-axis only at −0.25 and y-axis at ±0.5.

The constant gain loci are the following circles:

$$(k^2 - \frac{k}{U^2})y^2 = k(1 - \frac{x}{U})^2 - (1 - kx)^2, \tag{2.9}$$

on which $G_C = kU$. The centers of the circles are at

$$(x = \frac{U^2 - U}{kU^2 - 1}, y = 0),$$

and their radii are:

$$R = \frac{\sqrt{k + \frac{1}{kU^2} - \frac{2}{U}}}{k - \frac{1}{U^2}}.$$

These loci intercept the stability boundary at:

$$x = \frac{(kU)^2 - 2kU^2 + 1}{2k^2U - 2(kU)^2},$$

and the horizontal axis at:

$$\frac{U(1 \pm \sqrt{k})}{kU \pm \sqrt{k}}.$$

Finally, mapping a two-port network with a unilateral power gain of U to the gain plane by calculating its coordinates ($x = Re(U/A), y = Im(U/A)$), we can find on which gain locus it lies:

$$k = \frac{1 + 2x - \frac{2x}{U} + \frac{x^2+y^2}{U^2} - \sqrt{(1 + 2x - \frac{2x}{U} + \frac{x^2+y^2}{U^2})^2 - 4(x^2 + y^2)}}{2(x^2 + y^2)}, \tag{2.10}$$

where $G_C = kU$.

CHAPTER 3

A SYSTEMATIC METHOD FOR OPTIMUM MM-WAVE LNA DESIGN

3.1 Introduction

Mm-wave frequency range has become attractive in recent years for different applications [47] including high data rate communication [48–51], automobile radar [52–54], security and surveillance [55, 56] and imaging [57–60]. In this frequency range, the 94 GHz band specifically is gaining attention for the imaging application since the atmosphere attenuations at this band is one of the lowest in mm-wave frequency range (known as atmospheric window) which is an important factor for imaging [61]. This vast attention is a result of the possibility of low-cost mm-wave circuit implementation due to the significant progress in the silicon device fabrication [62].

This opportunity in turn demands developing methods for optimum mm-wave circuit design to have high performance systems. In fact, despite the appealing applications in mm-wave frequencies, the challenges in circuit design in this frequency range make it hard to achieve high performance systems. Namely, as frequency goes higher, U of the active device degrades [1]. This affects the activity of the device significantly and hence achieving high power gain becomes challenging. Moreover, the higher loss of the passive components such as transmission lines (TL's) at this frequency range makes the issue more severe [63]. In addition, considering the noise performance, as operation frequency goes higher, the noise of the transistors and also passive components (due to higher loss) increases. As a result, achieving low noise circuit at mm-wave is a challenging task to do.

Most of the systems employed in the mm-wave frequency applications have a re-

ceiver chain which requires an Low Noise Amplifier (LNA) as the first stage after antenna. Since usually the received signal is weak and the noise level of the environment is comparable to this signal, LNA has a crucial role in the chain to maintain the sensitivity of the system in the required range specified in the standard which means keeping the total NF of the system low by providing sufficient gain while introducing small amount of noise [10]. But considering the challenges stated above in the circuit design at mm-wave frequencies, i.e. higher loss and noise and lower activity, designing an LNA with low noise and high power gain is a hard goal to achieve and demands a robust design method to attain the high performance LNA.

There have been many reported mm-wave LNA's particularly at 94 GHz band fabricated in both SiGe and CMOS processes. In [64], a 91 GHz LNA with 5.3 dB noise figure, 32 dB power gain and 36 mW dc power consumption in a 28 nm CMOS process is reported which utilizes six cascode stages. A 92 GHz LNA with 5.7 dB NF and 27 dB gain is fabricated in a 0.25 μm InP/Si BiCMOS process which has 19.2 mW dc power consumption and four common emitter stages [65]. Having 6 dB NF and 10.7 dB gain, the LNA in [66] consumes 52 mW dc power and has three common source stages implemented in a 45 nm CMOS. In [67], four common emitter stages as LNA is fabricated in a 0.13 μm SiGe which shows 7 dB NF and 17.2 dB gain while consuming 24 mW dc power. The single stage cascode LNA reported in [68] has 8.6 dB nise figure and 9 dB gain implemented in a 0.13 μm BiCMOS with dc power consumption of 13 mW.

Although LNA is a principal block in the receiver chain, there is no established Figure of Merit (FoM) in the filed to fairly compare different LNA's performances and design methodologies. While NF and power gain are the main factors in LNA design, other effective factors should be considered in FoM to have a fair comparison between different methods and their ability to fully utilize the employed process capability in

generating power gain and low noise performance. First, the noise performance of different processes are different and some are inherently noisier than the others. Therefore, it is not fair to compare the design methods while not capturing the process effect on the performance. For instance, one LNA may show lower NF from the other one just because the employed process in the former is less noisy than the latter and if the second method is fabricated in first process, it would result in much better noise performance that the first LNA. The other effective parameter to be involved in the FoM is dc power consumption since having higher power gain in high frequency is usually a direct function of dc power. For instance, cascading the amplifier stages which is a common way to achieve higher power gain in mm-wave frequency range [64, 65, 67] directly shows itself in dc power consumption. Therefore, a definition for the LNA FoM is required to fairly compare the efficacy of design method in extracting high power and low noise regardless of the employed process. In this chapter, an FoM is proposed that captures the effect of these factors in LNA design.

While having high performance LNA at mm-wave frequencies is inevitable, there is only one known systematic method specifically proposed for LNA design [69]. It employs two inductors in the base/gate and emitter/drain of the main transistor to do the noise matching and power matching at the same time. In the next section, this conventional method is fully studied with the main focus on the mm-wave frequency range and it is shown that it is not the optimum design at high frequency considering the main factors in LNA circuit (NF and gain). A new methodology for optimum high frequency LNA design is presented in this chapter that finds the passive embeddings to be connected to the active device such that the resultant circuit achieves the optimum LNA performance and fully utilizes the capability of the employed process.

In this chapter, the conventional design method is reviewed and its drawbacks specif-

ically at high frequency are discussed. Then the new systematic LNA design method is proposed and based on that a 91 GHz LNA is designed wich shows 9.7 dB gain, 5.6 dB NF while consuming 6.3 mW dc power. This LNA achieves a very low FoM compared to state of the arts and to show the capability of the proposed method in fully utilizing the process potentials for LNA design. The conclusion part summarizes this work.

3.2 Conventional LNA Design Method

In order to gain insight into LNA design and realizing the need for a new design method which is systematic and optimum for the purpose of having LNA in a chain, it is beneficial to study the conventional LNA design method. First, the theory of this method is explained and then its issues mainly at high frequencies are discussed.

3.2.1 Theory

The purpose of this design method is to employ some embeddings in order to achieve simultaneous noise and power matching at the input. Assume an inductive degenerated transistor as in Fig. 3.1. Using the small signal model shown in the same figure, the input impedance of this circuit is derived as:

$$Z_{in} = j\omega L_e + \frac{1}{j\omega C_b} + L_e\omega_T, \tag{3.1}$$

where $\omega_T = \frac{g_m}{C_b}$. An interesting point of this equation is that the real part of Z_{in} is a function of L_e and it can be set to 50 Ω by selecting $L_e = \frac{50}{\omega_T}$.

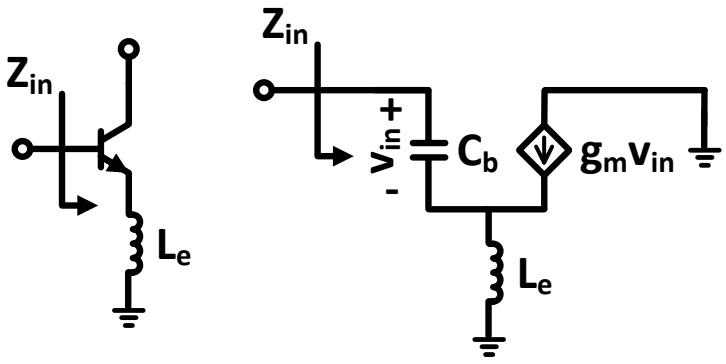

Figure 3.1: Inductive degenerated transistor and its low frequency small signal model

In order to examine the noise matching for this circuit, assume that the selected transistor has optimum source impedance of $R_{s,opt} + jX_{s,opt}$. It is shown in [9] that by connecting L_e to the transistor, the optimum source impedance of the circuit can be estimated as $R_{s,opt} + j[X_{s,opt} - L_e\omega]$. In other words, the real part of the optimum source impedance does not change. It is a significant feature since $R_{s,opt}$ of a transistor can be set to be 50 Ω by choosing the proper bias and size for the transistor [70]. That is, first the optimum current density which leads to the minimum F_{min} at the desired frequency in the given process is chosen [69]. Then, the transistor size is selected such that the corresponding $R_{s,opt}$ of the device becomes 50 Ω while maintaining optimum current density.

The imaginary part of Z_{in} is set to zero by adding an inductor (L_b) at the input of the circuit as demonstrated in Fig. 3.2. From (3.1), the proper value for L_b is:

$$L_b = \frac{1}{\omega^2 C_b} - L_e \tag{3.2}$$

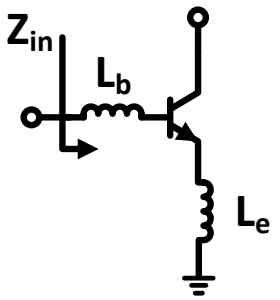

Figure 3.2: L_b is added to the circuit to set $Im(Z_{in}) = 0$

The optimum noise impedance of the circuit in Fig. 3.2 can be estimated by $R_{s,opt} + j[X_{s,opt} - \omega(L_b + L_e)]$ which means adding L_b to the circuit does not change $R_{s,opt}$. Also setting L_b to the value in (3.2) makes the overall $X_{s,opt}$ of the circuit to be zero [9]. Therefore, the imaginary parts in both input impedance and optimum source impedance become zero at the same time by setting L_b to the value in (3.2).

To summarize the conventional method for LNA design, first the optimum current density at which F_{min} of the device becomes minimum is selected. Then, the size of the transistor is chosen such that $R_{s,opt}$ of the device becomes 50 Ω. Having the size and bias, L_e and L_b are set to the values in (3.1) and (3.2) respectively to have both noise and power matching at the same time.

Though this design method is very effective in low frequencies, it does not result in an optimum design as the operation frequency increases. In the following, the drawbacks of this method with main focus on the high frequency performance are explained.

3.2.2 Drawbacks

The main issue with this method is that it has four generally independent parameters (R_{opt}, X_{opt}, $Re(Z_{in})$ and $Im(Z_{in})$) to be set in order to have simultaneous noise and power matching but there is only three degrees of freedom (transistor size, L_e and L_b) provided by the proposed structure. Therefore, the simultaneous noise and power matching cannot be done generally except for the cases that at least two of four parameters are not independent from each other. Indeed, in this method it is assumed that adding L_b to the circuit sets both X_{opt} and $Im(Z_{in})$ to zero based on the estimation used in deriving X_{opt} which means these two parameters are not independent. However, this is not the general case that happens in all circuits. The main equation is studied in the following to show that in high frequencies this does not happen.

Assume the configuration in Fig. 3.3. Using feedback equations in [9], the expression for the optimum source impedance of the whole structure can be found as :

$$R_{opt,tot} = \sqrt{(Re(\frac{Z_{cor,tran}+B}{C}))^2 + \frac{R_{u,tran}}{|C|^2 G_{n,tran}} + D}$$
$$X_{opt,tot} = -Im(\frac{Z_{cor,tran}+B}{C}) - L_e\omega, \tag{3.3}$$

where $Z_{cor,tran}$ is the noise correlation impedance of the transistor, $G_{n,tran} = \frac{\overline{I_n^2}}{4KT\Delta f}$, $R_{u,tran} = \frac{\overline{V_u^2}}{4KT\Delta f}$ and

$$C = \frac{z_{21,tran}}{z_{21,tran} + jL_e\omega}, \quad B = \frac{jL_e\omega(z_{21,tran} - z_{11,tran})}{z_{21,tran} + jL_e\omega}, \quad D = |\frac{\frac{Z_{cor,tran}+B}{C} + B - Z_{cor,tran}C}{C}|^2$$

in which $z_{ij,tran}$ is the z-parameter of the transistor.

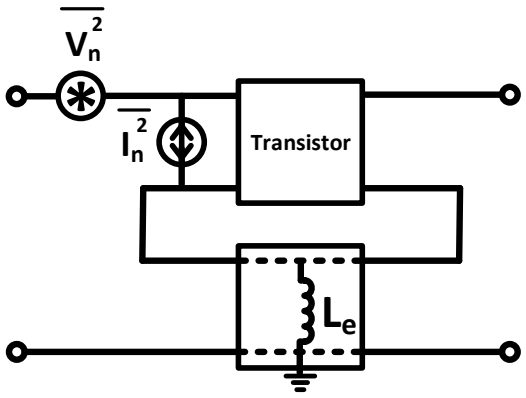

Figure 3.3: Two-port demonstration of the noisy transistor degenerated by L_e

If $L_e = \frac{50}{\omega_T}$ to make $Re(Z_{in}) = 50\Omega$, then:

$$B = \frac{j50\frac{\omega}{\omega_T}(z_{21,tran} - z_{11,tran})}{z_{21,tran} + j50\frac{\omega}{\omega_T}}, \quad C = \frac{z_{21,tran}}{z_{21,tran} + j50\frac{\omega}{\omega_T}}. \tag{3.4}$$

At low frequencies, specifically $\omega << \omega_T$, B and $|C|$ can be approximated by 0 and 1 respectively. It is the assumption utilized in conventional method to be able to approximate the total optimum source impedance as $R_{opt,tran} + j[X_{opt,tran} - \omega(L_b + L_e)]$ and justify the theory based on that.

At high frequency, the assumption of $\omega << \omega_T$ is not held and as it is evident form (3.4), B and $|C|$ take the values apart from 0 and 1 respectively. Figure 3.4 plots $|C|$ vs. frequency for a BJT in a 0.13 μm process which clearly shows that $|C|$ starts to drop and deviate from 1 as operation frequency increases. Therefore, assuming that adding L_e does not change $R_{opt,tot}$ is not correct at high frequency design. Also, setting L_b to the value of (3.2) which results in power matching does not result in noise matching at the same time since in high frequency $X_{opt,tot}$ is deviated form its low frequency value due to the variations in B and C. This means $X_{opt,tot}$ and $Im(Z_{in})$ are independent parameters at high frequency and setting one to zero does not necessarily set the other one to the desired value at the same time.

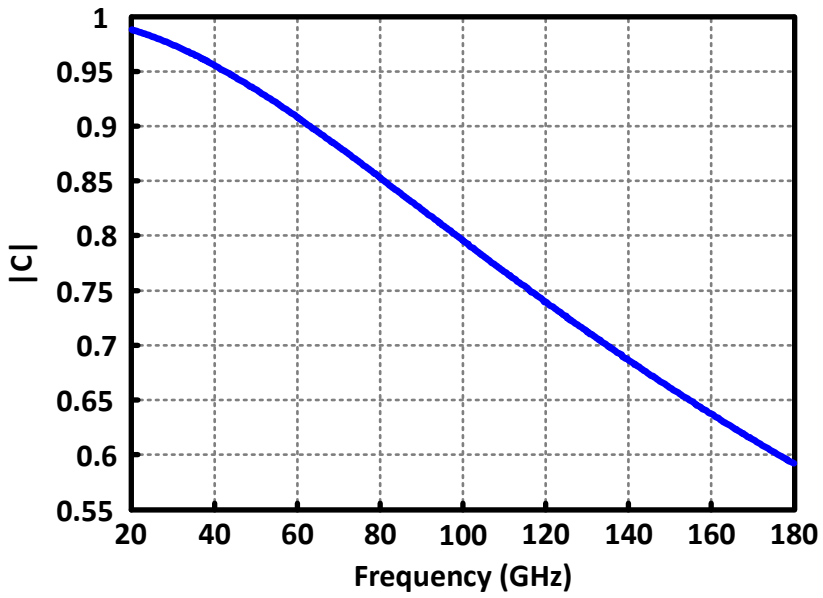

Figure 3.4: $|C|$ vs. Frequency for a BJT transistor in a 0.13 μm process

The other problem of the conventional method is that it assumes a unilateral device ($C_{bc} = 0$ in the small signal model of Fig. 3.1) which is again a reasonable assumption at low frequency but not at high frequency. When the circuit is not unilateral, the input impedance depends on the output matching network when the load is connected to the output via matching network. This fact will make finding L_e an iterative process if not impossible rather than a systematic way. Even considering a cascode device to make isolation between input and output does not help effectively and Z_{in} of the circuit in Fig. 3.1 would be a complicated function of C_{bc} [71]. Hence, finding the desirable L_e requires solving higher order equations or sweeping the value of inductor which is not a systematic method.

The other issue regarding conventional LNA design method is that the only factor targeted to enhanced in the design process is the noise figure. There is no mechanism to control and improve the gain. This approach works in low frequency since the device is

very active and the adequate power gain can be achieved without using optimum circuit. But at high frequencies, having sufficient power gain itself is a challenge and without a robust design method, this cannot be achieved. While this method is not considering power gain in the LNA design process, the total NF of the chain is a strong function of power gain of the first stage as shown in Friis' equation. Even having a very low noise LNA does not necessarily lead to low NF_{tot} of the chain without enough gain. Again, this approach is working for low frequencies but not a reasonable method for high frequency design. Indeed, the conventional method is not optimum for LNA design since it only considers noise factor rather than the main parameter which includes both noise factor and power gain. This parameter is introduced in the next section and a design method targeting this factor is proposed.

3.3 Noise Measure (M)

The concept of employing an LNA as the first stage in the chain is mainly a result of Friis' equation which shows noise and gain of the the first stage have critical role in determining the total noise of the chain. During the time, this subject was simplified to only considering the noise of the LNA and developing ways to design LNA's with low NF. This approach is directly resulted from LNA design in at low frequencies since high power gain can be easily achieved at those frequency ranges and it is not a concern. In this approach, it is assumed that NF of the chain would follow the noise performance of the LNA since the provided gain by LNA is high enough to suppress the noise of subsequent stages. But this assumption is not valid in high frequencies at which having adequate gain out of the amplifier itself is a challenge. Hence, to have a general and complete criterion for LNA design which considers both noise and gain in the circuit design, ***Noise Measure (M)*** introduced [7] which is directly derived from Friis' equa-

tion and addresses the main purpose in using LNA in the chain. In the following this parameter is thoroughly studied.

Suppose two gain stages are available with F_i and $G_{c,i}$ as noise factor and power gain respectively. There are two possible order for cascading these stages which one of them is shown in Fig. 3.5. Using Friis' equation, NF of each cascading order can be written as:

$$\begin{aligned} F_{12} &= F_1 + \frac{F_2 - 1}{G_{c,1}} \\ F_{21} &= F_2 + \frac{F_1 - 1}{G_{c,2}}, \end{aligned} \tag{3.5}$$

in which F_{ij} is NF of the cascaded order in which stage i is placed first.

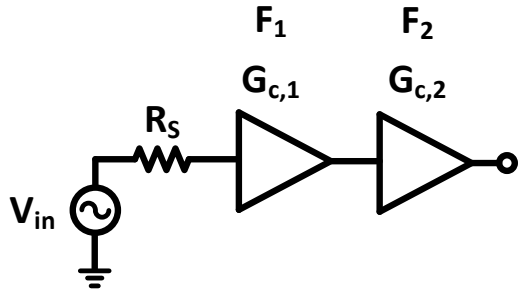

Figure 3.5: One possible cascading order of two gain stages

The question is which cascading order is the optimum one considering the NF of the chain. To derive a criterion, assume the order in Fig. 3.5 is the one that leads to the lower NF.i.e.$F_{12} < F_{21}$. Therefore:

$$\frac{F_1 - 1}{1 - \frac{1}{G_{c,1}}} < \frac{F_2 - 1}{1 - \frac{1}{G_{c,2}}}. \tag{3.6}$$

Equation (3.6) reveals that in a cascaded system of gain stages, the best order of cascading to have lower NF is to place first the one that has the lowest value of not F,

in contrary to common belief, but:

$$M = \frac{F-1}{1-\frac{1}{G_c}}. \tag{3.7}$$

This parameter is called ***Noise Measure (M)*** [7] and is the factor that should design for in an LNA rather than F in order to have lowest total NF of the system. Indeed, low M in first gain stage results in low NF_{tot} based on Friis' equation. Therefore, the main idea of the proposed method is to present a structure and solution that minimizes M and results in the optimum LNA circuit.

3.4 Noise in Two-Port Network Combinations

The purpose of this part is to find the equivalent noise input referred current ($I_{n,tot}$), input referred voltage ($V_{n,tot}$) and correlation admittance ($Y_{cor,tot}$) of the different combinations of two-port networks. These equations are necessary in defining noise parameters of the proposed structure and finding the optimum embedding using them such that a circuit with minimum M is achieved.

Cascade Combination

Cascade combination of two noisy two-port networks is depicted in Fig. 3.6. The equivalent noisy two-port network can be shown as Fig. 1.4 with y-parameters equal to the y-parameters of cascaded system.

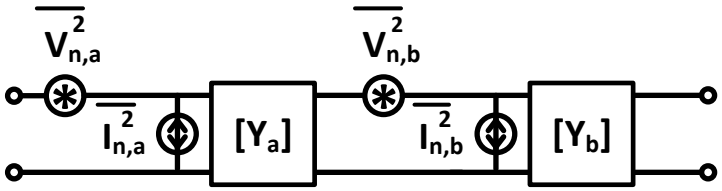

Figure 3.6: Cascade combination of two noisy two-port networks

To find $V_{n,tot}$, the inputs are assumed to be shorted in both systems in Figs. 3.6 and 1.4. The outputs can be connected to any passive lossless load. For simplicity, they are assumed to be shorted and i_{out} is derived in terms of y-parameters and the noise sources in each case. Since the two networks are equivalent, $V_{n,tot}$ can be found by equating i_{out} calculated for each one. This procedure results in:

$$i_{out} = -Y_{21}V_{n,tot} = -\frac{y_{21,b}}{y_{11,b} + y_{22,a}}(I_{n,b} + y_{22,a}V_{n,b} - y_{21,a}V_{n,a}), \tag{3.8}$$

where Y_{21} is the y-parameter of the equivalent network and is written as $\frac{y_{21,a}y_{21,b}}{y_{11,b}+y_{22,a}}$. Equation (3.8) can be solved to derive $V_{n,tot}$ in a cascaded system:

$$V_{n,tot} = \frac{1}{y_{21,a}}(I_{n,b} + y_{22,a}V_{n,b} - y_{21,a}V_{n,a}). \tag{3.9}$$

Hence, the voltage power noise is derived using (3.9) as:

$$\overline{V_{n,tot}^2} = \frac{1}{|y_{21,a}|^2}(\overline{I_{n,b}^2} + |y_{21,a}|^2\overline{V_{n,a}^2} + (|y_{22,a}|^2 + 2Re(y_{cor,b}y_{22,a}^*))\overline{V_{n,b}^2}). \tag{3.10}$$

$I_{n,out}$ is calculated assuming the open circuit at the inputs of the two-port networks while outputs are shorted which results in:

$$i_{out} = -\frac{Y_{21}}{Y_{11}}I_{n,out} = -\frac{y_{21,b}}{y_{11,a}(y_{11,b+y_{22,a}})-y_{12,a}y_{21,a}} \times \tag{3.11}$$

$$(y_{11,a}I_{n,b} - y_{21,a}I_{n,a} + (y_{11,a}y_{22,a} - y_{12,a}y_{21,a})V_{n,b}),$$

Where $Y_{11} = y_{11,a} - \frac{y_{21,a}y_{12,a}}{y_{11,b}+y_{22,a}}$. Solving (3.11) for $I_{n,tot}$ leads to:

$$I_{n,out} = \frac{1}{y_{21,a}}(y_{11,a}I_{n,b} - y_{21,a}I_{n,a} + (y_{11,a}y_{22,a} - y_{12,a}y_{21,a})V_{n,b}). \tag{3.12}$$

The total current noise power is derived using (3.12) as:

$$\overline{I^2_{n,tot}} = \frac{1}{|y_{21,a}|^2}(|y_{11,a}|^2\overline{I^2_{n,b}} + |y_{21,a}|^2\overline{I^2_{n,a}} + \tag{3.13}$$

$$(|y_{22,a}y_{11,a} - y_{12,a}y_{21,a}|^2 + 2Re(y_{cor,b}y_{11,a}(y_{22,a}y_{11,a} - y_{12,a}y_{21,a})^*))\overline{V^2_{n,b}}). \tag{3.14}$$

The next step is to find the noise correlation admittance ($Y_{cor,tot}$) which can be readily calculated using (1.13) and having $I_{n,out}$ and $V_{n,out}$:

$$Y_{cor,tot} = \frac{y_{11,a}\overline{I^2_{n,b}}+\overline{V_{n,b}}^2((y_{11,a}y_{22,a}-y_{12,a}y_{21,a})(y^*_{cor,b}+y^*_{22,a})+y_{11,a}y_{cor,b}y^*_{22,a})}{\overline{I^2_{n,b}}+|y_{22,a}|^2\overline{V^2_{n,b}}+|y_{21,a}|^2\overline{V^2_{n,a}}+2Re(y_{cor,b}y^*_{22,a})\overline{V^2_{n,b}}} + \tag{3.15}$$

$$\frac{|y_{21,a}|^2 y_{cor,a}\overline{V^2_{n,a}}}{\overline{I^2_{n,b}}+|y_{22,a}|^2\overline{V^2_{n,b}}+|y_{21,a}|^2\overline{V^2_{n,a}}+2Re(y_{cor,b}y^*_{22,a})\overline{V^2_{n,b}}}.$$

Parallel Combination

Parallel combination of two noisy two-port networks is depicted in Fig. 3.7. The strategy for finding equivalent noise parameters are similar to what described in cascade combination part. Using the shorted input networks, $V_{n,tot}$ is derived to be:

$$V_{n,tot} = \frac{y_{21,f}V_{n,f} + y_{21,a}V_{n,a}}{Y_{21}}, \tag{3.16}$$

where $Y_{21} = y_{21,a} + y_{21,f}$ and the total voltage noise power is found as:

$$\overline{V^2_{n,tot}} = \frac{1}{|Y_{21}|^2}(|y_{21,f}|^2\overline{V^2_{n,f}} + |y_{21,a}|^2\overline{V^2_{n,a}}). \tag{3.17}$$

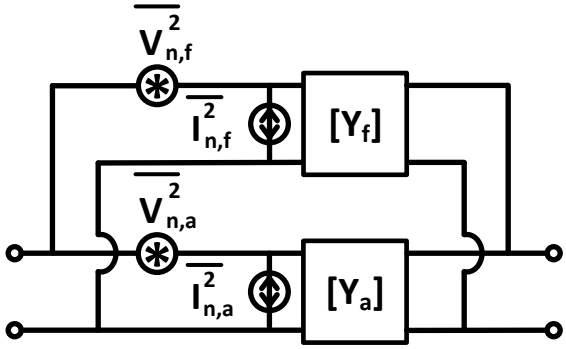

Figure 3.7: Parallel combination of two noisy two-port networks

The input referred noise current is calculated when the inputs are open:

$$I_{n,tot} = \alpha V_{n,a} + \beta V_{n,f} + I_{n,a} + I_{n,f}, \tag{3.18}$$

where

$$\alpha = \frac{y_{11,f}y_{21,a} - y_{21,f}y_{11,a}}{Y_{21}}, \quad \beta = \frac{y_{21,f}y_{11,a} - y_{21,a}y_{11,f}}{Y_{21}}. \tag{3.19}$$

The total current noise power is derived as:

$$\overline{I^2_{n,tot}} = \overline{I^2_{n,a}} + \overline{I^2_{n,f}} + (|\alpha|^2 + 2Re(y_{cor,a}\alpha^*))\overline{V^2_{n,a}} + (|\beta|^2 + 2Re(y_{cor,f}\beta^*))\overline{V^2_{n,f}}. \tag{3.20}$$

The noise correlation admittance ($Y_{cor,tot}$) can be calculated using (1.13) and $I_{n,out}$ and $V_{n,out}$ as:

$$Y_{cor,tot} = \frac{(y_{cor,f} + \beta)D_f^*\overline{V^2_{n,f}} + (y_{cor,a} + \alpha)D_a^*\overline{V^2_{n,a}}}{|D_f|^2\overline{V^2_{n,f}} + |D_a|^2\overline{V^2_{n,a}}}, \tag{3.21}$$

where $D_a = \frac{y_{21,a}}{Y_{21}}$ and $D_f = \frac{y_{21,f}}{Y_{21}}$.

Although the derived equations for noise parameters in cascade and parallel combinations are complicated, but they are essential in defining a mathematical model of the circuit and find the optimum solution for the defined model that achieves the optimum design. This approach is discussed in the following.

3.5 Proposed Structure and Systematic Method

In this section, a new systematic LNA design method is presented. Examining the structures in the published works, it is evident that there is no optimum systematic methodology to design LNA in mm-wave frequencies and one cannot make sure that the resultant circuit is the optimal one in the given process. This fact brings the attention to the need for a method of mm-wave LNA design and gives the motivation to study the subject profoundly to come up with an efficient solution.

Considering the input referred power noises derived in (3.10), (3.13), (3.17) and (3.20), it is evident that the total referred noise can be made lower or slightly higher than the noise of the original network by proper selection of networks connecting to it. This means combinations of embeddings can be found such that the noise of the system does not increase significantly or even decreases. Figure 3.8 shows the noise factor for an embedded device using lossless embeddings in a 0.13 μm process such that resulting noise factor (F) is significantly lower than F_{min} of the transistor. This example shows the potential of utilizing embeddings in the design to enhance noise performance of the circuit.

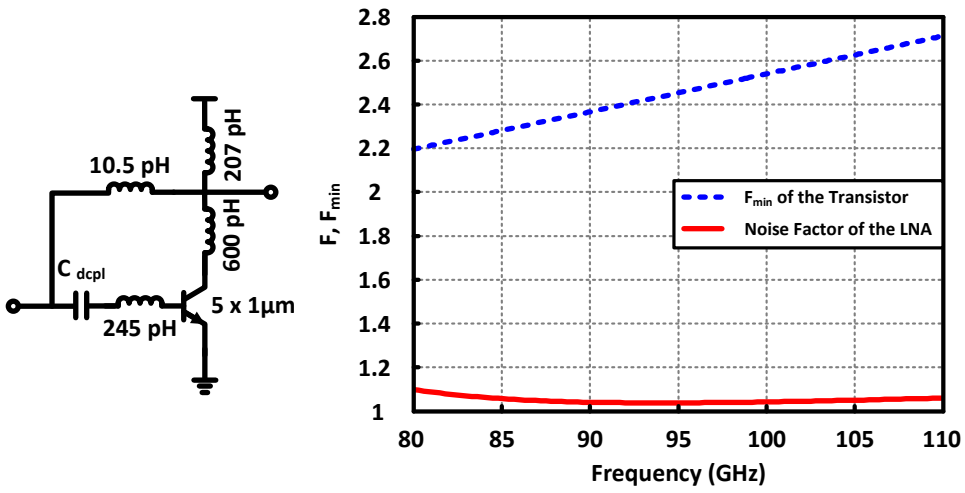

Figure 3.8: Noise factor of the embedded device and F_{min} of the device in a 0.13 μm process

This is a significant point since it means noise of the system can be optimally shaped by proper embeddings. The same behavior is reported for G_c, i.e. embeddings can be employed to enhance it [72]. Therefore, the proposed method is to employ the general form of the embeddings around the active core as shown in Fig. 3.9 and find the optimum values of them such that noise measure (M), which is function of G_c and F, for the resultant circuit becomes minimum while the stability of the amplifier is assured. This

is feasible since the embeddings connected to the transistor are capable of changing both noise and power gain. In fact, finding the optimum embeddings that do not significantly increase the noise of the circuit and at the same time lead to high power gain and hence minimum M is the main strategy of this method.

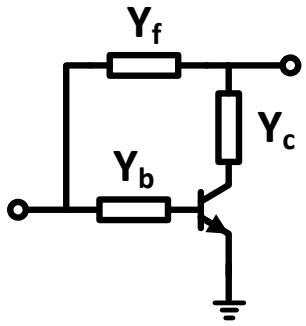

Figure 3.9: Proposed structure for systematic optimum LNA design

It is worth mentioning that when the embeddings are lossy and noisy, having F smaller than F_{min} is not happening for practical values of them but still they can be found such that the minimum increment in the total noise occurs. The circuit in Fig. 3.8 also reveals this important fact that considering only noise factor for designing an LNA is not a correct approach since though F of the circuit is significantly low but the gain of the amplifier is slightly higher than 1 which make it pointless to use in system.

The next step toward optimum LNA design is establishing a way to find optimum values for the components. It is clear from the structure in Fig. 3.9 that the active device is cascaded with Y_b and Y_c and the resultant network is in parallel with Y_f. Assuming all the components are noisy and using the derived equations in the previous section, the equivalent noise parameters are calculated for each combination. After deriving the noise and y-parameters of the whole structure, F and G_c and hence M of the network can be found as a function of y-parameters and noise characteristics of the active device and

the embeddings. Having the active device size and bias, the design task is completed by finding the optimum values for Y_f,Y_b and Y_c. This can be done using a constrained optimization solver since the circuit has been modeled by a cost function problem, i.e. finding variables Y_f,Y_b and Y_c such that M becomes minimum. In other words, the circuit design is mapped to a parametric optimization problem defined as:

$$\min_{Y_f,Y_b,Y_c} \{M\}$$

such that:

$$\frac{U}{A} \in \text{Convex Stability Region of (2.3)}$$

One way of solving this problem is to write the equations derived for the structure in a code in MATLAB and use optimization solvers compatible with this software. Creating the code file in MATLAB is simple and can be done once and used for all LNA designs afterwards which justifies that the proposed method is systematic.

The defined problem is a nonlinear one and needs a solver that exploits efficient techniques to be able to solve it. The optimization solver SNOPT [40] is used in this work which is one of the efficient ones and capable of solving this problem and giving the optimum values. After attaining the optimum values, the circuit is implemented using these values in the proposed structure.

To summarize the proposed systematic design method, the main steps toward the optimum design are:

1. Select the proper device size and bias (explained in the next section)
2. For the proposed structure in Fig. 3.9, find the noise and y-parameters in terms of the active device and embeddings parameters using equations derived in section

3.4.

3. Write F and G_c for the structure employing the equations in (1.10) and (1.16) and the results of the previous step.
4. Calculate $M = \frac{F-1}{1-\frac{1}{G_c}}$.
5. Find optimum values which result in minimum M while assuring stability of the whole circuit. This can be done using an optimization solver by defining M as the cost function and the stability boundary derived in (2.3) as the constraint in a given range for embedding values.
6. implement the circuit using the optimum values.

It is worthwhile mentioning that since the results of steps 2 to 4 are in general from and parametric, once prepared, they can be used for future LNA design which means there is no need to repeat these steps for them. The procedure explained above is a general guideline for the optimum LNA design. Next section explains more details about the design steps stated above by designing a 91 GHz LNA in a 0.13 μm process employing this method.

An important point to cover before starting the design is deriving the noise factor of the network considering the SCM condition as shown in Fig. 3.10 which is utilized in defining M is step four.

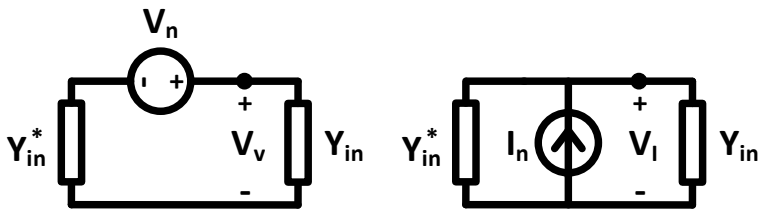

Figure 3.11: Circuit for calculating voltage at the input of the two-port network due to noise sources

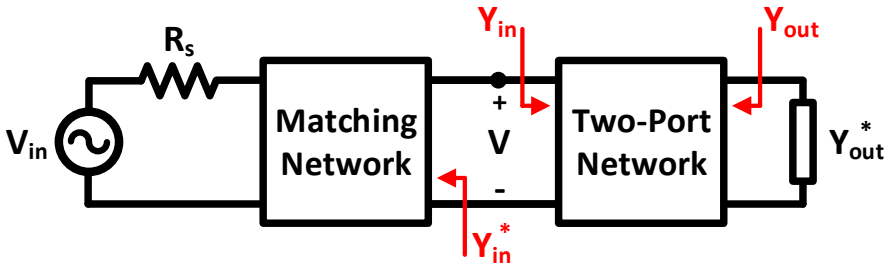

Figure 3.10: Two-port network in SCM condition connected to the source

To do so, the voltage at the input of the two-port network caused by each source is calculated and then noise factor of the structure would be readily derived using the definition of that. The voltage at the input port due to current and voltage noise sources are derived using circuit in Fig. 3.11 as:

$$V_V = \frac{Y_{in}}{Y_{in} + Y_{in}^*} V_n \tag{3.22}$$

for the voltage noise source and

$$V_I = \frac{I_n}{Y_{in} + Y_{in}^*} \tag{3.23}$$

for the current noise source. The voltage gain from source to the input of the two-port network considering lossless input matching is $\sqrt{\frac{G_s}{4g_s}}$ [71] in which g_s is real part of Y_{in}

and G_s is real part of source admittance ($\frac{1}{50}$ in this design). Therefore, the noise factor of the network assuming lossless conjugate input matching is derived as:

$$F = 1 + \frac{I_n^2 + V_n^2(|Y_{in}|^2 + 2Re(Y_c Y_{in}))}{4KTg_s} = 1 + \frac{G_n + (|Y_{in}|^2 + 2Re(Y_c Y_{in}))R_n}{g_s}. \quad (3.24)$$

3.6 Design Example: A 90 GHz LNA

In this part, using the presented systematic method, a 91 GHz with 5.6 dB NF and 9.7 dB power gain which consumes 6.3 mW dc power is designed and implemented in a 0.13 μm SiGe process with f_T/f_{max} of 220/280 GHz [41]. In order to calculate the total noise parameters of the structure, noise parameters of the active and passive embeddings should be known. Therefore, first the general form of the noise parameters of active and passive devices are derived in order to develop the optimization code for the proposed structure. Then, the optimum bias and size for the transistor is selected and using its noise and y-parameters as the input to the optimization solver, the optimum passive embeddings are achieved. The simulation results along with the layout of the circuit are shown at the end of this section.

3.6.1 Determining Noise of Active and Passive Components

To obtain the input referred noise sources of the transistor, the method described in 3.4 is employed in Cadence. To be specific, in the simulation setup, the output of the transistor is shorted as ac ground. The setup for finding voltage input referred noise is depicted in Fig. 3.12. The output current which is due to the noise is found by running a noise analysis. Then, an ideal ac voltage source is connected to the input and an ac analysis is run to find the voltage to current gain of the transistor. The voltage input referred noise

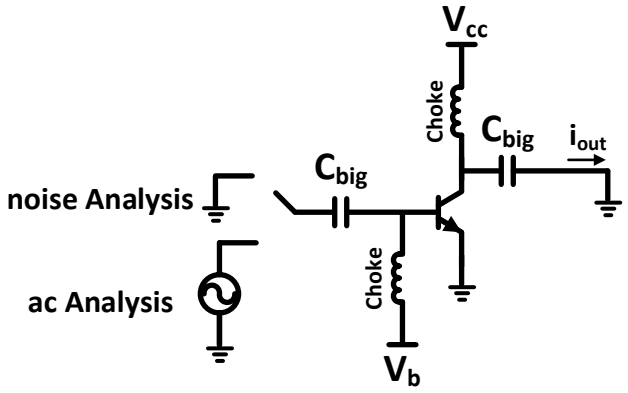

Figure 3.12: Setup for noise and ac analysis in Cadence to derive the input referred voltage noise of the transistor

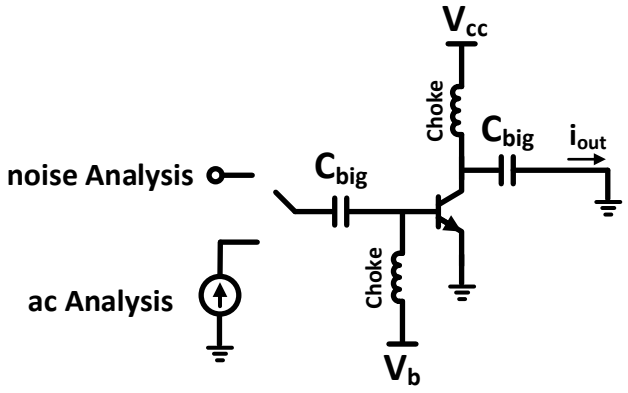

Figure 3.13: The setup for noise and ac analysis in Cadence to derive the input referred current noise of the transistor

is obtained by dividing the former by the latter.

The setup to attain current input referred noise is shown in Fig. 3.12. A noise analysis is run while the input is open circuit to find output current due to the noise of the transistor. Next, an ideal ac current source is connected to the input to find current gain of the transistor using ac analysis. The input referred current noise is then achieved by dividing the output current noise by this current gain. The next step to complete

the noise characterization of the transistor is to derive the correlation admittance of the device. Assuming the two dominant noise sources in a BJT are shot noise in base-emitter ($\overline{i_{b,n}^2}$) and collector-emitter ($\overline{i_{c,n}^2}$) junctions, using the definition in (1.13) and the equations in [73] and [74], the correlation admittance can be written as:

$$Y_{cor,tran} = \frac{1}{\overline{V_{n,tran}^2}}(\overline{i_{c,n}^2}\frac{y_{11}}{|y_{21}|^2} + \frac{\overline{i_{b,n}i_{c,n}^*}}{y_{21}^*}) = \frac{1}{\overline{V_n^2}}(2qI_c\frac{y_{11}}{|y_{21}|^2} + 2KT(1 - \frac{g_{m_0}}{y_{21}^*})), \tag{3.25}$$

where $\overline{V_{n,tran}^2}$ is voltage input referred noise of the transistor, I_c is the collector bias current, K is Boltzmann constant, q is the electrical charge of the electron, T is temperature in Kelvin and g_{m_0} is the low frequency limit of y_{21}. As it is evident from (3.25), even if $\overline{i_{c,n}^2}$ and $\overline{i_{b,n}^2}$ assumed to be uncorrelated, the voltage and current input referred noise sources are correlated and this correlation should be included in the noise calculation.

The noise of the passive components, i.e. transmission lines (TL's) and the capacitors, is due to the ohmic loss of their structure which is not negligible at high frequency. For each of these passive components, EM simulation in HFSS can be done to determine the loss. The noise of the element is then modeled by $4KTR_{loss}$ in which R_{loss} is series equivalent resistance and this can be used as the noise source of the element in the optimization. To include the noise contribution of the passive components in the simulation, Thermal Noise option of the N-port (that contains s-parameters of the EM simulation of the passive component) in the test bench in Cadence is activated which make the passive to be noisy considering its loss.

Based on the explanations and equations in this part and section 3.4, the total noise parameters of the proposed structure is formulated and the optimization code is written in general form to be used in systematic LNA design. The next step is to select the device bias and size as the active core of the circuit.

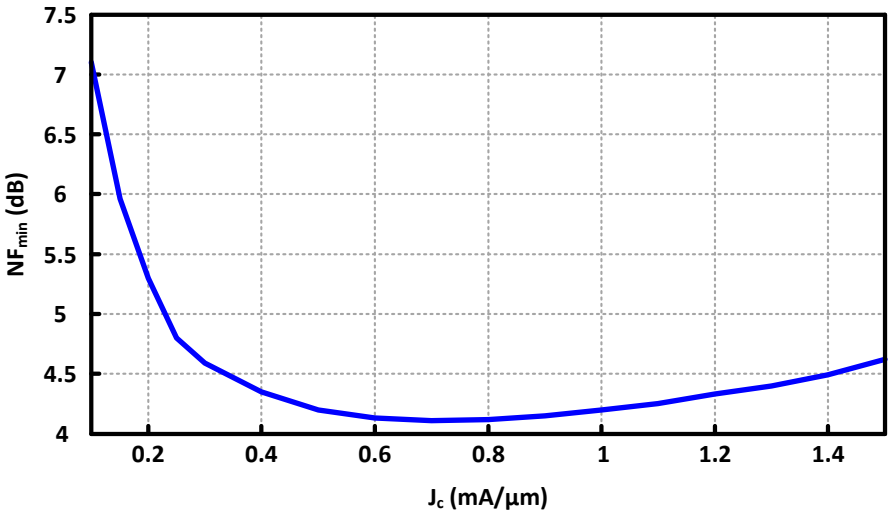

Figure 3.14: NF_{min} vs. collector current density (J_c) for a cascode BJT structure at 92 GHz in a 0.13 μm SiGe process

3.6.2 Transistor Size and Bias Selection

Device selection for LNA design is a crucial part since the dominant source of the noise in the circuit is transistor and it is important to select the bias and size that result in less noise. Moreover, since the gain is another factor to be considered in LNA, these parameters should be chosen in a way that the selected device is capable of providing enough gain and has reasonable activity.

In order to have sufficient gain, a cascode structure with identical transistors is utilized as the active core of the LNA. As shown in Fig. 3.14 there is an optimum collector current density which results in the minimum NF_{min} at the desired frequency. According to this plot, the optimum current density that the cascode pair in the employed process can be biased at, is $\sim 0.6\ mA/\mu m$. Also, note that for the current densities between 0.4 $mA/\mu m$ to 1.2 $mA/\mu m$, NF_{min} of the device increases less than 5% compared to its minimum value. This optimum current density range provides the flexibility in the size selection for higher power gain while controlling dc power consumption.

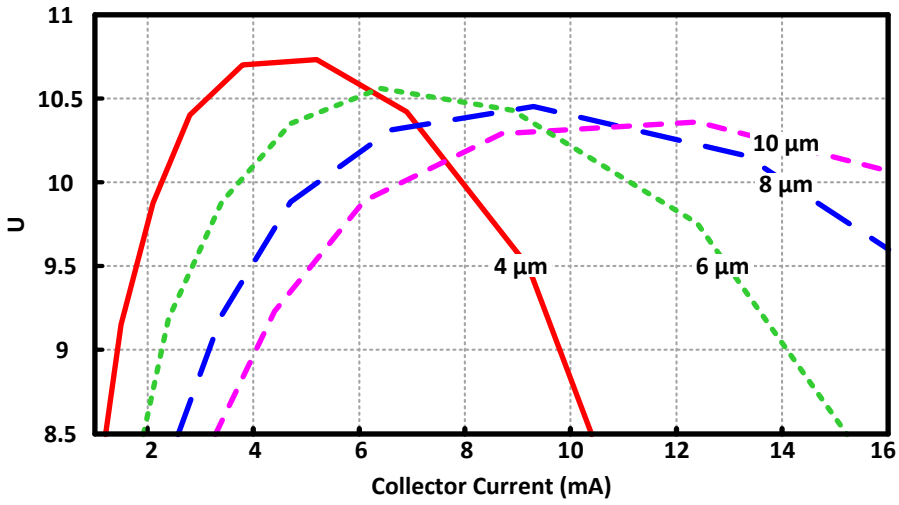

Figure 3.15: U vs. collector current in the BJT for different emitter lengths at 92 GHz in a 0.13 μm SiGe process

After choosing the current density based on the noise performance, the size of the transistor should be selected. This choice is a trade off between power gain and dc power consumption in one side and output power on the other side. Similar to power amplifier, setting the dc current to large values results in higher output power when designed properly but increases dc power. On the other hand, for each emitter length, there is an optimum collector current that results in maximum U as shown in Fig. 3.15 and hence highest power gain. Having the current density, the size of the transistor is selected using Fig. 3.15 considering this trade off. Higher U is achieved in smaller currents but in price of less output power. In this design, the size of the transistor is selected based on having sufficient gain and less dc power consumption since in LNA design usually power gain and dc power consumption are more important than capability in providing higher output power, the areas in left side of Fig. 3.15 are more desirable. Considering this fact and having current density, a size with large U which results in reasonable amount of dc current is selected.

In a cascode structure, however, U is not well-behaved and a plot like Fig. 3.15

cannot be achieved. In this case, the bias current is chosen based on dc and the current density selected in previous part based on noise performance. In this design, a power budget of 6 mW is assumed for the circuit with a power supply equal to 2 V. Selecting the current density as 0.5 $mA/\mu m$, the size of the transistor would be 6 μm. Employing fingers for the selected transistor slightly decreases parasitic resistance and capacitances which is beneficial for both noise and activity of the device and make them improve. Therefore, a transistor with maximum number of finger allowed in the process is chosen which leads to have 5×1.2 μm as the transistor size.

After the bias and size of the transistor is selected, its noise characteristics are found using methods and equations in section 3.6.1. This information along with y-parameters of the active device is used as the input to the optimization solver to find the optimum embeddings.

3.6.3 Passive Components Design

In order to have a sense about the type of the embeddings, i.e. capacitive or inductive, and hence designing the passive structures, the optimization can be run using ideal noiseless components. In this design, for the selected active core bias and size, the optimization solver results in inductive embeddings as the solution to the optimum LNA design when using ideal components in the optimization code. Therefore, a transmission line (TL) structure should be selected to serve as the inductive components. In this work, a Grounded Coplanar Waveguide (GCPW) structure (depicted in Fig. 3.16) is chosen to efficiently confine the electromagnetic wave inside the structure and isolate the signal line from the rest of the components in the circuit and minimize the coupling between them.

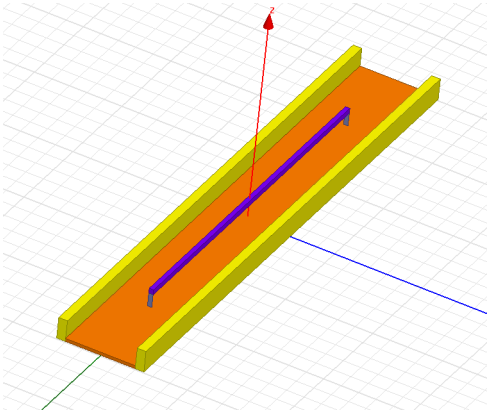

Figure 3.16: The GCPW structure utilized in the design

The wall to wall distance is desirable to be wide to have less capacitive parasitics between signal track and grounded walls. On the other hand, this distance cannot be arbitrary large for the sake of area and also implementation of the TL's where they are bending while their length is not too long. Therefore, a compromise between the parasitics and layout should be made. Considering this trade off, a wall distance of 40 μm is selected. The wall of the GCPW is made of all the layers from lower to top metal layer connected together to decrease the resistance of the path. The width of the walls are chosen to be 5 μm wide in order to allow the return current to pass through it with low resistance and loss. The ground plane underneath the signal track should be thick enough to decrease the resistance and far enough from the signal track to reduce the parasitics to the ground. Based on these trade offs, the three lower metals are stacked to form the ground plane while being 7.6 μm far from the signal track. The width of the signal track is selected considering the trade off between α and Z_0 where α is the real part of propagation constant and Z_0 is the characteristic impedance of the TL. In order to have the minimum loss, the width that results in minimum $|\frac{\alpha}{Z_0}|$ should be selected [36]. Fig. 3.17 shows $|\frac{Z_0}{\alpha}|$ for the employed GCPW with different signal track width which leads to chose 2.5 μm as the width of the signal path to have minimum loss in the TL at

94 GHz.

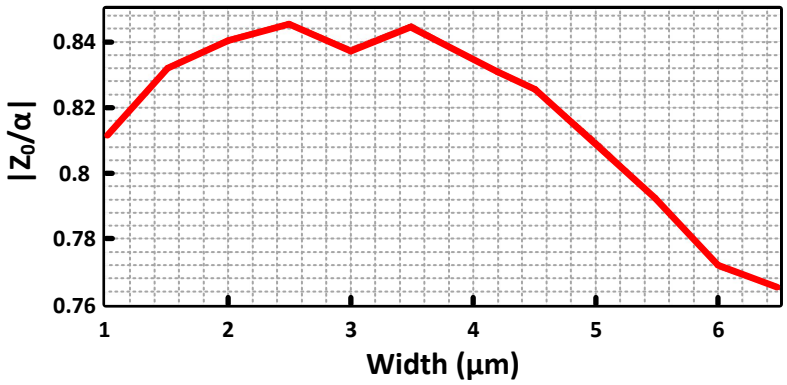

Figure 3.17: $|\frac{Z_0}{\alpha}|$ of the GCPW structure for different signal track width

An other passive component which is utilized in the design is the capacitor. The decouple capacitor should acquire small impedance and high quality factor (Q) at the operation frequency. Therefore, size of this capacitor would be relatively large in order to provide large capacitance. On the other hand, having large areas means introducing more resistance and loss and also more capacitive parasitics to the ground which degrade Q. In order to compromise between these two factors, i.e achieving large capacitance and the area, a finger cap structure is selected as shown in Fig. 3.18 which has more effective area in comparison to a simple two-plate capacitor because of the areas between the fingers. This means the same capacitance can be achieved with smaller lateral area which reduces the resistance and result in better Q. This structure is also beneficial for series capacitor in the matching network since smaller area leads to less parasitics to the ground and higher Q and thence better matching quality.

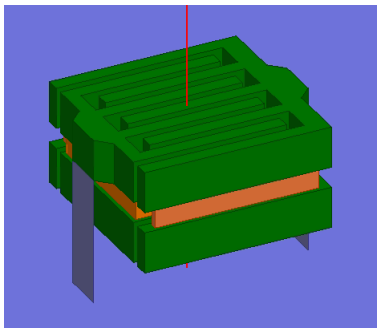

Figure 3.18: The finger capacitor structure to be employed as series capacitor

In order to minimize the parasitics to the ground top metal layers winch are far from the ground plane are selected. This layer choice also helps with the loss inside the structure top metal layers are much less lossy than other layers. In order to further decrease the loss of the structure, the two top metal layers are connected together to have thicker fingers and reduce the resistance while the distance to the ground plane is reasonably far. Having the capacitor plates at the top metal layers also helps to further enhance Q since it eliminates the need for employing vias because the signal track is at the same layer as the capacitor.

The capacitors which are connected to the ground at one port are used in the matching networks. The most important factor for this component is its Q since a lossy matching network degrades the noise figure and power gain significantly. In order to have a high Q capacitor with a plate connected to the ground, the signal plate is sandwiched between two other metal layers connected together as the ground plate to confine all the electromagnetic energy inside the structure and lower the parasitics. The three lower metals are selected to implement this capacitor as shown in Fig. 3.19 to provide the desired value for the capacitance with smaller area since the distance between these layers is very small.

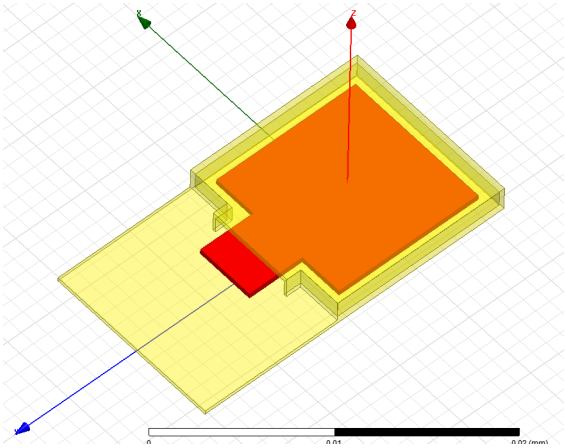

Figure 3.19: Capacitor structure for the matching network

3.6.4 Single Stage LNA

After selecting the device size and bias and the passive structures, the final step is to find the optimum values for the embeddings using actual models of passive components and implement the circuit. To run the optimization, the y-parameters and noise of the TL structure in a reasonable range considering the wavelength of the operation frequency is required as the data for the solver. Therefore, these information for TL's of length 1 μm to 400 μm are provided to the solver in the steps of 5 μm. The decoupling capacitor is designed using the finger-cap structure with 7 fingers of 0.6 $\mu m \times 29$ μm which shows 250 fF capacitance with Q equal to 25 around 90 GHz and a resonance frequency of 210 GHz which is far enough from the target frequency. the y-parameters of this component along with its noise is considered in the series with Y_{bc} in the code to includes its effect into the design.

The written code for the proposed structure employs y-parameters and noise characteristics of the selected transistor as the input and gives the optimum values for the

embeddings that results in minimum M while assuring stability of the circuit. Performing this optimization in MATLAB exploiting SNOPT [40] as the solver provides the optimum embeddings as:

$$TL_b = 121.4 \quad \mu m$$

$$TL_c = 140.6 \quad \mu m$$

$$TL_{bc} = 283.3 \quad \mu m$$

Employing these values in the structure using discrete straight TL's, results in NF of 4.9 dB and G_c equal to 10.8 dB and M equal to 2.28 while consuming 6 mW dc power considering perfect conjugate matching at the input and the output. It is worth mentioning that the optimum values above are for the straight TL's. In reality, the TL's have to bend and deviate from straight form because of layout and area limitations. Therefore, each TL as the embedding is EM simulated considering its geometry in the layout such that its y-parameters becomes as close as possible to the optimum embedding value. After finding the right length and shape for each TL, the whole structure is EM simulated to consider all coupling effects. Once the structure is finalized and the simulation results are close to the predicted ones, the input and output matching networks to have SCM circuit are designed to achieve maximum power flow in the input and the output. Since these matching networks introduce loss, the noise and gain performance of the circuit would be affected. Also, the pads are an inevitable part of the layout that should be considered in parallel with 50 Ω load. Both input and output pads are customized such that they become part of matching networks to make them as simple as possible. In order to make the circuit unconditionally stable under source and load connections, a series LC network is connected to the base with resonance frequency at 60 GHz to open the feedback loop and prevent the oscillation. This structure does not affect the circuit performance significantly at 90 GHz since its impedance is high enough to be considered

as open circuit at that frequency. The schematic of the single stage LNA with the values of each component is demonstrated in Fig. 3.20 and the layout of the circuit is shown in Fig. 3.21.

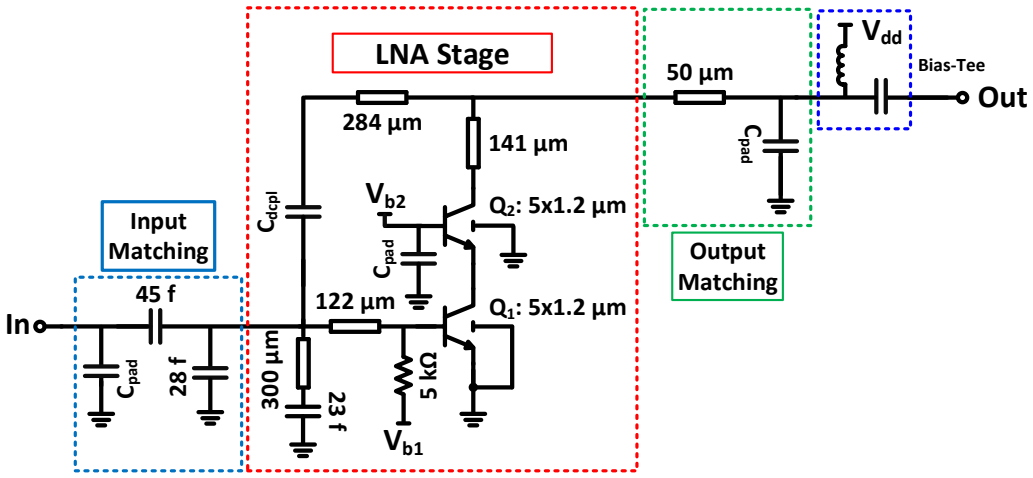

Figure 3.20: Schematic of the single stage LNA

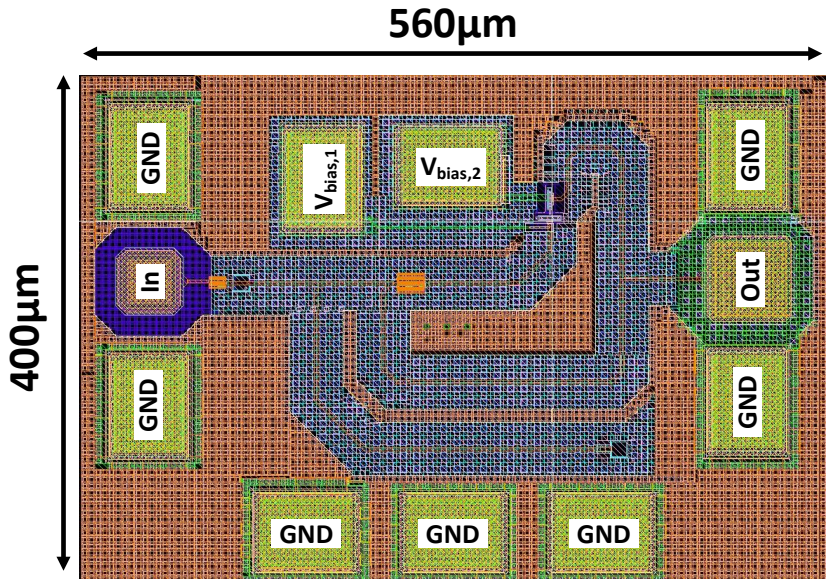

Figure 3.21: Layout of the single stage LNA in a 0.13 μm SiGe process

The LNA is simulated in Cadence using post layout models of the transistors and the

EM simulation result of the whole passive structure including vias, embeddings, pads and matching networks. It shows 5.6 dB noise figure and 9.7 dB gain at 91 GHz while consuming 6.3 mW dc power. The simulated S-parameters of the LNA is depicted in Fig. 3.22. Based on this plot, the 3-dB bandwidth of the circuit is 12 GHz. Figure 3.23 shows the large signal simulation results of the LNA which shows 1 dBm saturated output power.

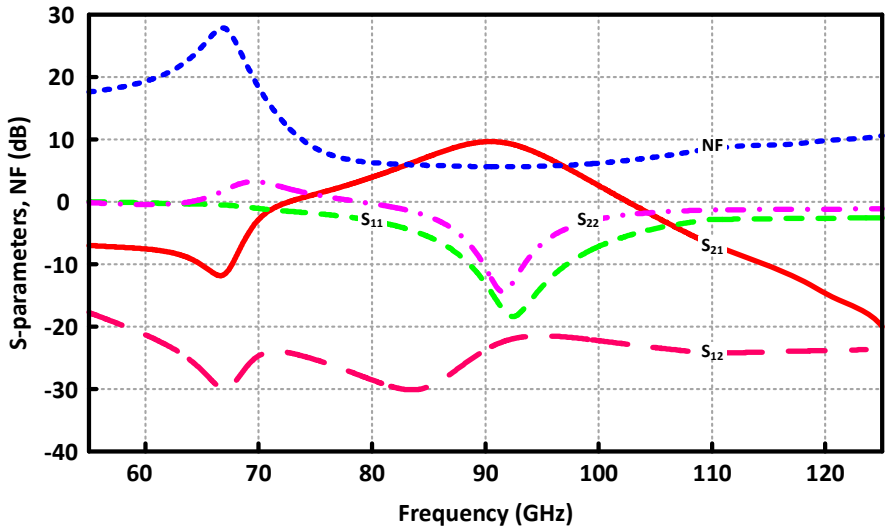

Figure 3.22: Simulated S-parameters and NF of the single stage LNA

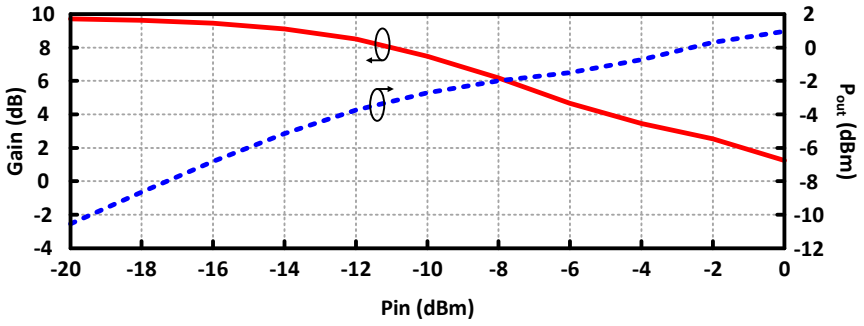

Figure 3.23: Simulated large signal behavior of the single stage LNA

In order to fairly compare different LNA performances in different processes, an

FoM is required which includes all the significant and effective factors. Unfortunately, there is no well-known FoM for LNA in the field despite its crucial role. In this part, an FoM for LNA is presented which considers main parameters and factors. As discussed before, noise factor (F) and power gain (G_c) are among important factors in LNA since they readily set the noise figure of the whole chain. Moreover, the noise performance of the transistor as the main noise source in the circuit is a strong function of the process. Namely, F_{min} of a transistor at frequency of f is a function of f/f_T [75, 76]. This means having a process with higher f_T results in having a less noisy active device at the frequency of interest. This concept is similar to the concept of f_{max} when considering activity of the device: having a process with higher f_{max} means more active device at the given frequency. Therefore, employing same design method to design two LNA's in two processes with different f_T results in different noise figures since one process is inherently more noisy that the other one. Hence, to capture the effect of the employed process in the noise performance of LNA to have a fair comparison between different design methods, it is legitimate to involve f/f_T into FoM. In addition, dc power consumption is an other important factor to be considered which shows itself in achieving high gain in an LNA (and hence improving M) by cascading some gain stages or biasing the transistor in high currents.

Indeed, the goal of the proposed FoM is to clarify how much dc power is burnt to achieve the reported power gain and NF while takes into account the role of the employed process in noise performance of the circuit to have a fair comparison for different LNA design methods. The proposed FoM is defined as:

$$\text{FoM} = 0.1 \times (\frac{P_{dc}}{1mW})(\frac{f_T}{f})(\frac{F-1}{1-\frac{1}{G_c}}). \tag{3.26}$$

Table 3.1 compares the performance of this design with the reported works which shows this LNA achieves very low FoM compared to the state of the arts and proves the

efficacy of the proposed method in extracting the noise and gain capability of the device to have high performance LNA.

Table 3.1: Comparison Table

	Process	**Freq.** (GHz)	**NF** (dB)	**Gain** (dB)	P_{dc} (mW)	**3-dB BW** (GHz)	f_T (GHz)	**M**	**FoM**
[77]	90 nm SiGe BiCMOS	90	5.1	19	43	30	290	2.27	31.4
[78]	65 nm CMOS	90	7	27	36	8	180	4	28.95
[79]	130 nm SiGe	91	6	45	19.2	24	220	2.98	14.45
[64]	28 nm CMOS	91	5.3	32	36	5	340	2.38	32.1
[65]	250 nm InP/Si BiCMOS	92	5.7	27.7	19.2	18	330	2.72	18.7
[80]	90 nm SiGe	94	4.2	10	8.8	20	300	1.81	5.1
[81]	90 nm SiGe BiCMOS	94	4.3	28	15.6	> 35	300	1.7	8.45
[67]	130 nm SiGe BiCMOS	94	7	17.2	24	8	250	4.1	26.1
[82]	130 nm SiGe	94	7.7	10.5	21.3	27	230	5.37	28
[82]	130 nm SiGe	94	7	5	11.2	> 30	230	5.87	16.1
[68]	130 nm SiGe BiCMOS	95	8.6	9	13	7	230	7.1	22.4
[66]	45 nm CMOS	95	6	10.7	52	18	300	3.26	53.5
This Work	**130 nm SiGe**	**91**	**5.6**	**9.7**	**6.3**	**12**	**220**	**2.95**	**4.49**

3.7 Conclusion

A systematic method for mm-wave LNA design is presented. The optimum passive embeddings in the proposed structure are found such that the noise measure ($\frac{F-1}{1-\frac{1}{G_c}}$) of the whole circuit is minimized. Based on this method, a 91 GHz single stage LNA is designed in a 0.13 μm SiGe process which achieves 9.7 dB gain, 5.6 dB NF and 1 dB saturated output power while consuming 6.3 mW dc power consumption.

CHAPTER 4

AN EFFICIENT HIGH POWER MM-WAVE VCO DESIGN METHOD

4.1 Introduction

Mm-wave frequency range spanning from 100 GHz to 300 GHz is gaining attention in today's technology due to attractive features such as see-through capability, non-ionizing radiation and available large bandwidth [19]. These features make this frequency range appealing for many applications such as imaging [83–85], safety and security [12, 14, 86] and high-speed communication [16, 17, 87].

Signal source is a crucial block in all the mm-wave applications which is required to generate sufficient amount of power at the output in an efficient way while providing reasonable tuning range. There are many mm-wave oscillators employing solid state devices in recent years due to increasing demand in mm-wave applications [88–95].

While efficient tunable high power signal source is desirable, there are some serious issues in mm-wave frequency range which makes it difficult to achieve these goals. As frequency increases, the activity of the active device decreases which means the device capability in generating power degrades [1]. Having higher loss in the passive structures such as TL's and capacitors at high frequency due to skin effect and working close to the resonance frequency of the structure worsens this problem [96]. Moreover, high loss in the varactors at mm-wave frequencies drastically affects the tunability of the oscillators in addition to lowering the out power and efficiency [88]. All these issues imply the significance of the an efficient method for mm-wave signal source design in order to efficiently extract the device capability in power generation while having mechanisms to tune the frequency effectively.

There are many reported signal sources working above 100 GHz which have utilized different structures and methods to enhance at least one of the main factors in this block, i.e. output power, DC-to-RF efficiency and tuning range. The highest DC-to-RF efficiency is reported for the oscillator designed in [97] with 25.9% which has 3.4 dBm peak output power at 177 GHz without tuning range fabricated in a 65 nm CMOS process. The highest peak output power is achieved in [63] which generates 6.5 dBm peak output power at 195 GHz while having 15.3 % best DC-to-RF efficiency and 1.1% tuning range in a 55 nm SiGe process. The widest tuning range is reported in [98] as 39.4% at center frequency of 107 GHz with -15 dBm peak output power and 1.1 % best DC-to RF efficiency in a 65 nm CMOS process. As it is clear from theses reported works, focusing on one parameter and enhance it significantly impacts the other factors severely and makes the designed work to be poor considering these factors.

In the next section, the existing methods for improving either power, efficiency and tuning range at high frequency is discussed. Then, a new method for mm-wave VCO design is proposed which achieves very high output power and efficiency while is capable of providing sufficient tuning range. Based on this method, A 110 GHz VCO is designed in a 55 nm SiGe which achieves 6.3 dBm peak output power, 20.9% DC-to-RF efficiency and 5.2% tuning range. This VCO has the highest peak output power at F and D band and highest DC-to-RF efficiency all reported SiGe/CMOS mm-wave oscillators. Finally, the conclusion section at the end of this chapter summarizes the work.

4.2 A review on Existing Methods for MM-Wave Source Design

There are two main approaches in high frequency oscillator design to extract output power at the desired frequency. The first one employs conventional structures such as

cross-coupled and Colpitts and tries to apply low frequency methods with some modification to make them compatible with high frequency. Working on passive structures to make them less lossy, careful layout or changing transistor size and bias to get higher power from the circuit are some of examples. A Colpitts structure is utilized in [99] to achieve 2.7 dBm output power at 106 GHz. In [100], a cross-coupled structure with LC tank is employed to design a VCO having -3.5 dBm peak output power at 115 GHz. This approach is not a systematic and there is no clear steps and guidelines toward oscillator design. In fact, it is the designer's art to somehow extract as high as possible power at the output. In addition, there is no assurance that the designed oscillator is fully utilizing the capability of the device or the design process is on the right road toward the maximum power extraction.

While the most desirable condition is being able to directly maximize output power (P_R) by employing a new method or structure, the problem is that this power is a function of network electrical variables (as derived in (1.2) and these parameters cannot be set employing linear techniques since they are results of nonlinear procedure in the oscillator. Therefore, in the second approach, there has been long lasting research in oscillator design to find a function or parameter that can be optimized in order to improve the power generation in the circuit and may get close to the desired goal. In some of the works, a power related function was defined and conventional or new structures are utilized to achieve higher output power. In [94], the optimum conditions to maximize $\frac{P_R}{|V_{in}||V_{out}|}$ are derived based on which two ring oscillators at 104 GHz and 121 GHz, employing some embeddings to provide the conditions, were designed showing -2.7 dBm and -3.5 dBm peak output power respectively in a 65 nm CMOS process. In [63], maximally efficient power gain (G_{ME}) is maximized using new structure to have high output power and efficiency. A 195 GHz VCO is designed using this method which shows 6.5 dBm output power and 15.3% efficiency and 1.1 % tuning range in a 55 nm SiGe pro-

cess. In other work, U of the structure, as the measure of activity of two-port networks, is maximized and shaped at the desired frequency employing passive embeddings in new structure to boost the power gain and efficiency. A 175 GHz oscillator is designed utilizing this method which achieves 4.8 dBm output power and 11.7% efficiency with 0.34% tuning range in a 130 nm SiGe process. These methods are systematic and very efficient in generating and extracting power at the desired frequency but poor in providing tuning range.

To design oscillators with sufficient tuning range at high frequency, many different ideas have been employed. Some high frequency works try to design a high Q varactors with reasonable C_{max}/C_{min} in the conventional or new structure to tune the frequency. In [101], accumulation mode varactors are utilized in Colpitts structure to provide 7.8 % tuning range at the center frequency of 118 GHz and -14 dBm output power and 0.71 % efficiency in a 65 nm CMOS process. Some other works came up with new ideas to tune the frequency by employing coupled oscillators and controlling the phase shift between them. The work in [88] employs both varactors and coupled oscillators and gains wider frequency tuning. This VCO achieves 9.5 % tuning range at center frequency of 105 GHz with 4.5 dBm output power and 5.3 % efficiency in a 65 nm CMOS process. In [92], an inductive structure is employed to tune the frequency to eliminate the varactor and avoid the effect of its loss on power and tuning. It shows 3.5 % tuning range while having -7.2 dBm output power and 0.64 % efficiency in a 0.13 μm SiGe process. The parasitic capacitance of the transistor and their dependency on the bias voltage are exploited in some works to tune the frequency. Using this technique, VCO in [102] achieves 8.7 % tuning range with -1 dBm output power and 3.7 % efficiency in a 65 nm CMOS process. Some works utilize mode switching mechanisms to have wide tuning range. The VCO in [103] achieves 20.7% tuning range at frequency of 190 GHz and while providing -2.1 dBm peak output power. As it is evident from the reported works,

having wide tuning range with high output power and efficiency is a hard goal to achieve and new methods and structures are required to have a high performance VCO at high frequency. In next section, a new method and structure is proposed which results in high power and efficiency while being capable of providing sufficient tuning range. It is note worthy that the ideas of getting high tuning range at low frequency usually do not work at higher frequency. Most of the ideas at low frequency work on the inductor since the loss in the inductors is the limit for tuning range where as at high frequency the loss of varactors is the limit.

4.3 Proposed Method and Structure

In this section, the basic idea of the efficient high power VCO design is presented and based on that a systematic method and a structure to employ it are proposed. An oscillator can be considered as a network which delivers some portion of the generated power by the active device to the load and feeds back the remaining to the input to sustain power generation as shown in Fig. 4.1. From this point of view, at a given bias point and frequency, the desired oscillator is the one that delivers the highest power to the load (P_L) which is a portion of the generated power in the active device (P_{out}) by sensing the input power fed back from output to the input (P_{in}). Therefore, this power (P_L) is related to those other two powers and defining a function capturing this fact can be a right target for efficient high power oscillator design.

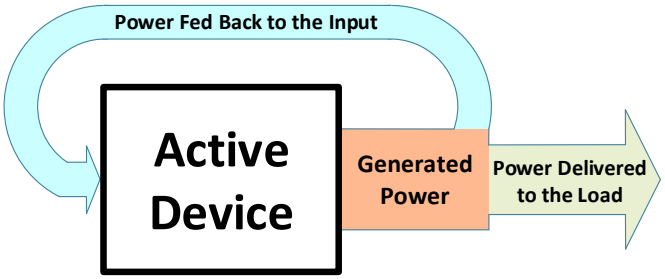

Figure 4.1: Concept of power flow in an oscillator

Based on this power flow, it is legitimate to define a new power gain that includes P_L and P_{in}. This power gain, $G_{p,osc}$, is defined as:

$$G_{p,osc} = \frac{P_L}{P_{in}}, \tag{4.1}$$

where P_L is delivered power to the load and P_{in} is the input power of the active device. This power gain has a significant difference from operating power gain (G_p) of two-port networks. P_{in} in G_P is an external source connected to the input and generates power at the output and is independent of that. However, in $G_{p,osc}$, this power is not independent from output and this fact shows itself in deriving its formula in the following. Therefore, this power gain has a different name than G_p to emphasis on this point. Maximizing this power gain results in high power and efficient oscillator since the intention in the definition of this gain is to deliver the highest portion of the generated power in the active device to the load for the given DC power consumption. In order to be able to maximize this quantity, optimum embeddings around the active device and the specific load should be employed. Since different embeddings have different roles in determining the voltage and currents and hence the power of the two-port network, the proposed structure utilizes the general form of embeddings as depicted in Fig. 4.2. In general, the embeddings can be inductive or capacitive depending on the employed process.

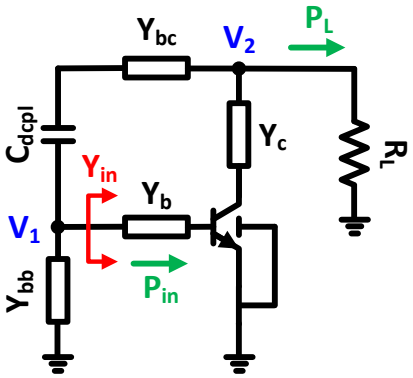

Figure 4.2: Proposed structure for efficient oscillator design

The next step is to define $G_{p,osc}$ in terms of y-parameters of the device, embeddings and the load to find the optimum values which result in maximum $G_{p,osc}$. Considering the variables shown in Fig. 4.2 and using the definition of $G_{p,osc}$, one can derive:

$$G_{p,osc} = \frac{g_L|V_2|^2}{g_{in}|V_1|^2} = \frac{g_L}{g_{in}}|a|^2, \tag{4.2}$$

where $a = \frac{V_2}{V_1}$ and $g_{in} = Re(Y_{in})$ and g_L is the load admittance. The quantity of a can be written in terms of the admittances of the components in the proposed structure as:

$$a = 1 + \frac{Y_{bb} + Y_{in}}{Y_{bc}}, \tag{4.3}$$

To find Y_{in}, the circuit in Fig. 4.2 can be considered as infinity numbers of the unit networks connecting together as shown in Fig. 4.3 which can be demonstrated as a terminated two-port network as shown in the right side in Fig. 4.3. Writing the input impedance equation for this terminated two-port network leads to:

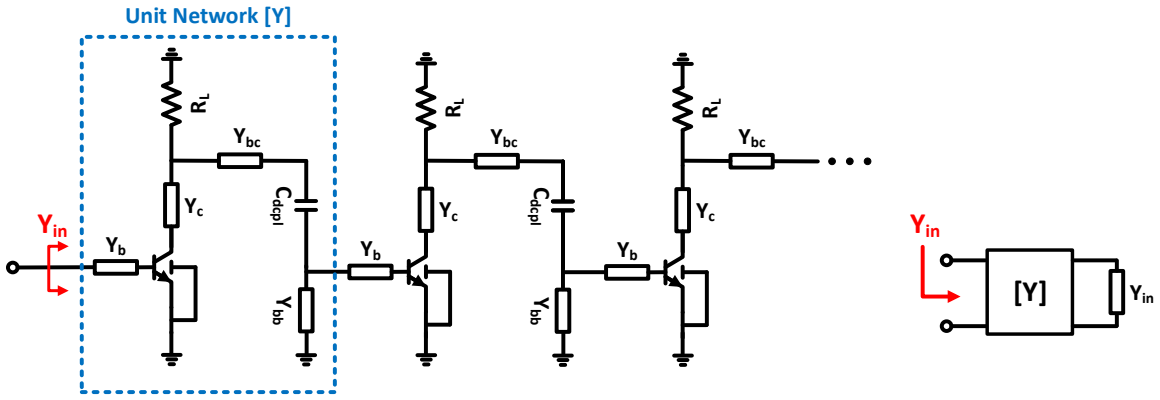

Figure 4.3: Circuit for calculating Y_{in} and the equivalent two-port network

$$Y_{in} = y_{11} - \frac{y_{12}y_{21}}{y_{22} + Y_{in}}, \tag{4.4}$$

in which y_{ij}'s are y-parameters of the unit network in Fig. 4.3. Y_{in} is calculated by solving (4.4) which results in:

$$Y_{in} = 0.5(y_{11} - y_{22} + \sqrt{(y_{11} + y_{22})^2 - 4y_{12}y_{21}}). \tag{4.5}$$

Hence, a can be expressed in terms of y-parameters of the network substituting Y_{in} in (4.3) with the term in right side of (4.5). Therefore, G_{osc} is derived as a function of network parameters as:

$$G_{osc} = \frac{g_L}{g_{in}}|1 + \frac{Y_{bb} + Y_{in}}{Y_{bc}}|^2 = \frac{g_L}{g_{in}}|1 + \frac{Y_{bb} + 0.5(y_{11} - y_{22} + \sqrt{(y_{11} + y_{22})^2 - 4y_{12}y_{21}})}{Y_{bc}}|^2, \tag{4.6}$$

in which g_{in} is the real part of Y_{in} or equivalently the derived impedance in (4.5).

Since G_{osc} is written in terms of y-parameters of the network consisting of active device, load and the embeddings, it can be used as the cost function to be maximized by finding optimum embeddings and the load in th proposed structure. In order to design

the structure as an oscillator, its instability should be assured by moving the network outside of the stability region in (1.10). Also, since the oscillator should be able to give power to the load, the real part of the output impedance should be negative at the desired frequency to make sure that it is delivering power to the load. This output impedance is calculated by disconnecting R_L and looking into the circuit in Fig. 4.2 from the output port. On the other hand, the real part of Y_{in} should be positive in order to absorb the power fed back from the output to sustain the oscillation. Theretofore, an optimization problem is defined such that G_{osc} is the cost function and the three mentioned conditions are the constraints to be satisfied:

$$\max_{Y_b, Y_{bb}, Y_{bc}, Y_b, R_L} \{G_{osc}\}$$

such that:

$$\frac{U}{A} \notin \text{Convex Stability Region of (2.3)}$$

$$Re(Y_{in}) > 0$$

$$Re(Y_{out}) < 0$$

The solution to this optimization problem results in optimum embeddings and the load that achieve high oscillator power gain while making sure of the oscillation of the structure at the desired frequency. Having the structure of the oscillator, the y-parameters of the whole circuit can be written in terms of the series and parallel combinations of the components. Utilizing the y-parameters of the whole structure, the required functions for optimization, i.e. G_{osc} for performing maximization, U and A for defining stability boundary and Y_{out} and Y_{in} to be used in two of the constraints, are defined. This constrained optimization problem is written as a code in MATLAB and exploiting SNOPT [40] as the optimization solver. The y-parameters of the active device is the input for the solver and it finds the solution to the problem in the provided range of the

values for the embeddings.

4.4 Design Example: A 110 GHz VCO

In this section, employing the proposed method, a 110 GHz VCO with 6.3 dBm peak output power, 20.9% best DC-to-RF efficiency and 5.2% tuning range is designed and implemented in a 55 nm SiGe process which achieves highest peak output power at F and D Band and highest DC-to-RF efficiency below $f_{max}/2$ among all reported SiGe/CMOS mm-wave oscillators.

4.4.1 Transistor and Passive Structures Selection

The first step of the design is selecting the transistor size and bias. Since the activity and capability in providing power gain of the device is related to its U [19], for each size, the desired collector bias current is the one that results in maximum U at the operation frequency. As shown in Fig. 4.4, there is an optimum collector current to achieve the highest U for a given emitter length. This optimum point occurs at higher bias currents for larger transistor with less sensitivity to changes in the current, i.e. the plot becomes more flat as the size of the transistor increases. Since the capability of the device to deliver high output power to the load is an important factor, higher bias current and hence larger device size is desirable. On the other hand, larger device means introducing more parasitics to the circuit. Therefore, there is a compromise between having larger device size and more parasitics on one side and higher optimum current and higher capability in delivering output power to the load and less sensitivity of U to the changes in the current on the other side. Considering this trade off, a device with emitter length of

13 μm biased at 10 mA bias current is selected in this work that has tolerable parasitics in the target frequency and high optimum collector current. After choosing the total emitter length, the number of fingers are found such that highest U is achieved. Hence, a transistor with 2×6.5 μm is selected to be used as the active core of this design.

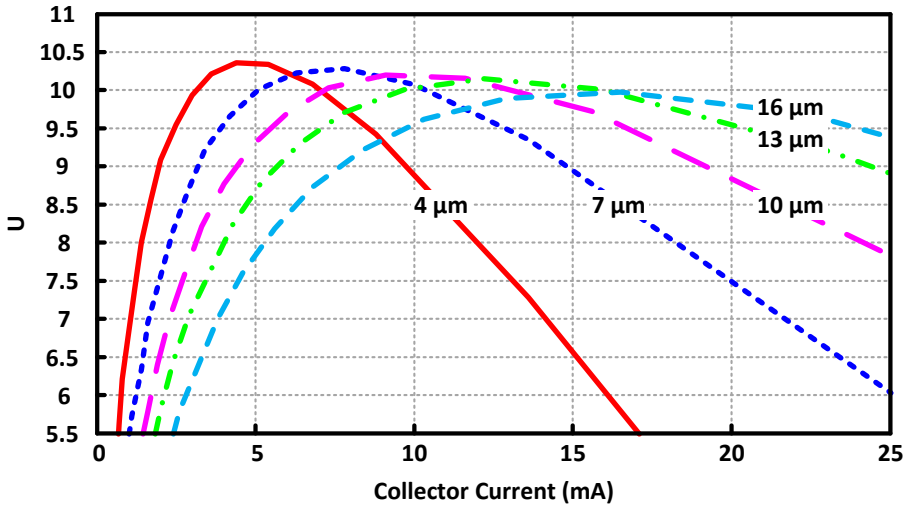

Figure 4.4: U vs. collector current in the BJT for different emitter lengths at 115 GHz in a 55 nm SiGe process

To define the presented optimization problem, the structure of the passives which will be employed in the design should be determined. Since almost all the embeddings are inductive in this process and hence realized by TL's, it is important to choose the structure and the dimensions for TL's with minimum loss. Since in high frequency coupling to other components in the design has a significant effect in wasting the electromagnetic energy, Grounded Coplanar Waveguide (GCPW) structure is utilized to confine all this energy inside the structure which is shown in Fig. 3.16. The wall-to-wall distance is chosen such that the parasitic capacitance from signal track to the walls become negligible. The walls are made from stacked seven layer metals in order to decrease the loss by thickening the path. The ground plane is made of the low metal layers to maintain the highest distance from the signal track to decrease the parasitics to

the ground which is 5.7 μm in this process. This plane is a patterned low metal stacked to the substrate to reduce the loss of the ground by providing huge number of vias to connect them. The signal track size is selected to have minimum $|\frac{\alpha}{Z_0}|$ [36] where α is the real part of propagation constant and Z_0 is the characteristic impedance of the TL. Based on all these considerations, a GCPW with 2.5 μm signal track width and 30 μm distance between the walls is employed in this design.

The decoupling capacitor is designed as a finger cap with six fingers of 13.5 $\mu m \times$ 0.6 μm in top metal layers in order to provide high density capacitor per area and less parasitics to the ground. The two top metal layers are stacked together to form the fingers in order to thicken the metal and decrease the loss. These considerations results in high Q for such big capacitor. The decoupling cap shows 150 fF capacitance with Q around 20 and a resonance frequency close to 250 GHz which is far enough from the target oscillation frequency ($\sim$ 115 GHz). The capacitor for the matching is connected to the ground in one port and is fabricated using three lower metal layers in which the middle metal is sandwiched between other two layers as depicted in Fig. 3.19. This structure confines all the energy inside it and decreases the size of the plates which significantly increase Q of the capacitor.

4.4.2 Optimization and Implementation

After selecting the active device bias and size and the passive structures, the optimum embeddings can be found. The y-parameters of the transistor are the inputs to the solver to find the optimum embeddings for the selected device. The y-parameters of the TL's in a reasonable range, compared to the wave length of the operation frequency, are provided to the solver to find the optimum embeddings in that range. In this work, the

y-parameters of the GCPW's from 5 μm to 400 μm in steps of 5 μm is provided. The optimization solver gives the optimum embeddings for the selected device as:

$$TL_b = 8.9 \quad \mu m$$

$$TL_c = 2.7 \quad \mu m$$

$$TL_{bc} = 151.3 \quad \mu m$$

$$C_{bb} = 55 \quad fF$$

$$R_L = 183 \quad \Omega$$

The VCO is designed employing the optimum values in the proposed structure. TL_{bc} is a bending GCPW to form the feedback loop and C_{bb} is a varactor to tune the frequency. the dimension of this varactor is $6 \times 2.2\ \mu m \times 0.1\ \mu m$ which provides a capacitance between 30 fF to 67 fF as shown in Fig. 4.5. Figure 4.6 demonstrates $G_{p,osc}$ of the designed VCO which clearly shows that the optimum embeddings and the load, maximize the defined power gain at the desired frequency as it is expected.

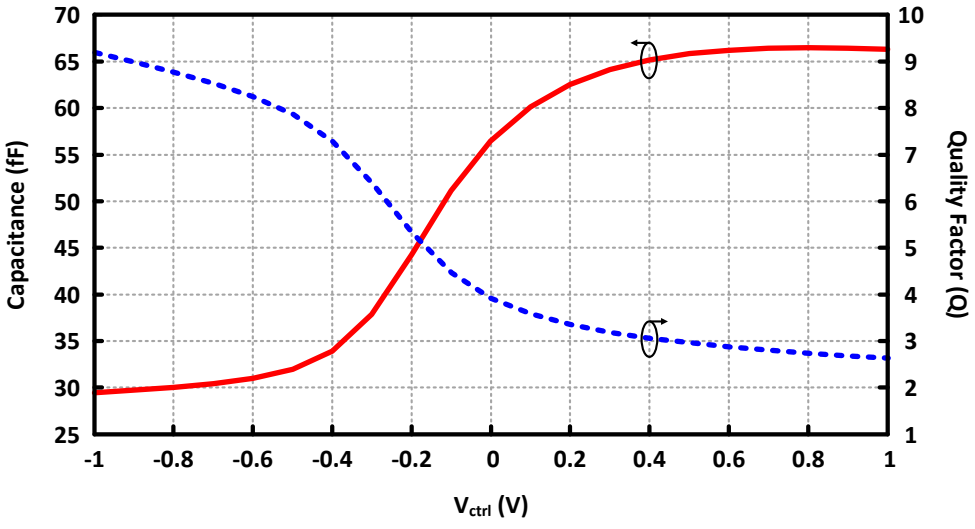

Figure 4.5: Capacitance and quality factor of a varactor with size of $6 \times 2.2\ \mu m \times 0.1\ \mu m$ at 115 GHz in a 55 nm SiGe process

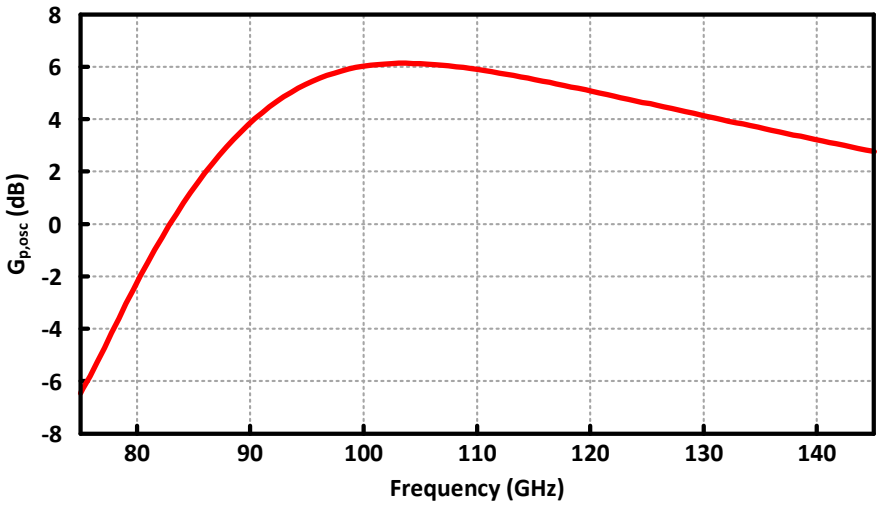

Figure 4.6: $G_{p,osc}$ of the designed VCO employing optimum load

The matching network to move 50 Ω to the optimum load, is a π-network that includes the pad capacitance. The output pad is costume designed in order to provide the proper capacitance value for the matching. The whole structure from vias to the pads are carefully EM simulated all together in HFSS in order to capture all parasitics and coupling effect. The complete schematic of the oscillator and the layout of the circuit are shown in Fig. 4.7 and Fig. 4.8 respectively.

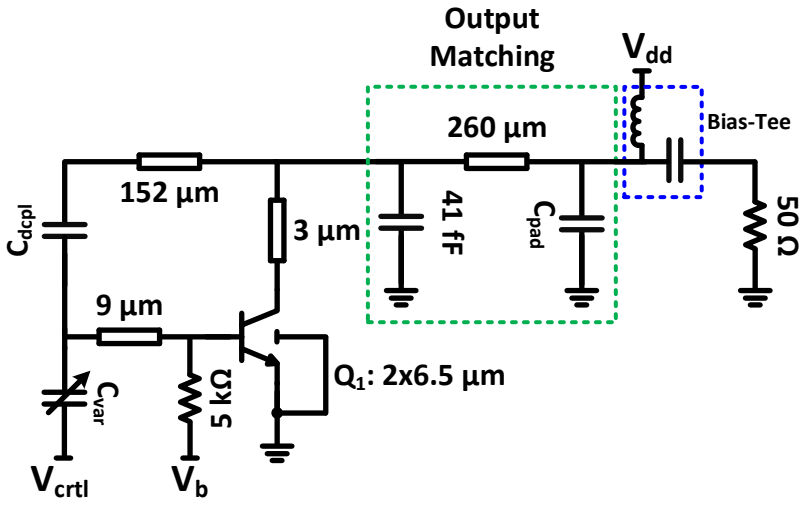

Figure 4.7: Complete schematic of the designed VCO in a 55 nm SiGe process

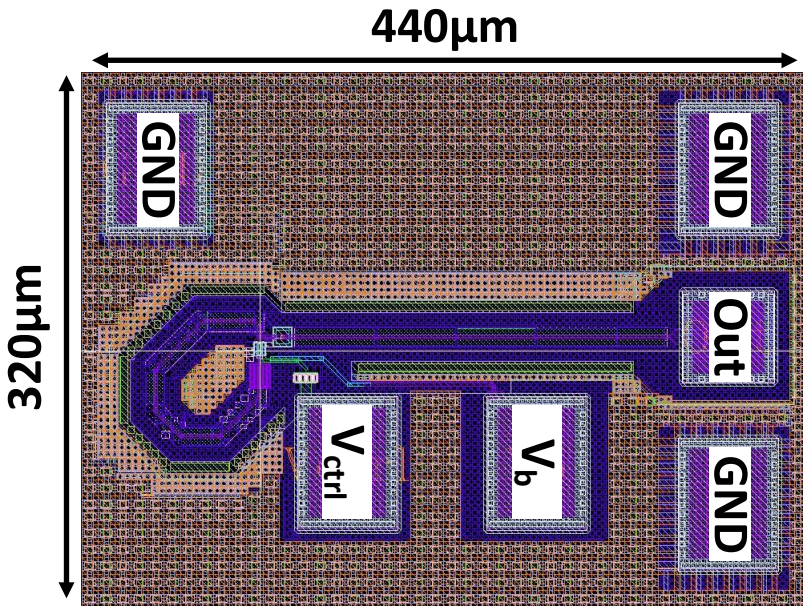

Figure 4.8: Layout of the designed VCO in a 55 nm SiGe process

The VCO achieves 6.3 dBm as peak output power while showing 19.3 % efficiency. The simulated output power is depicted in Fig .4.10 that justifies the proposed method in

extracting the power at fundamental frequency. The best DC-to-RF efficiency is 20.9% while consuming 16.9 mW dc power from a 1.7 V power supply. The frequency can be changed from 106.4 GHz to 112 GHz as shown in Fig .4.9 that results in 5.2% tuning range. Table 4.1 compares the results of this VCO with the state of the arts that shows this work achieves highest peak output power in F and D band and highest DC-to-RF efficiency below $f_{max}/2$ among all mm-wave VCO's in SiGe/CMOS processes.

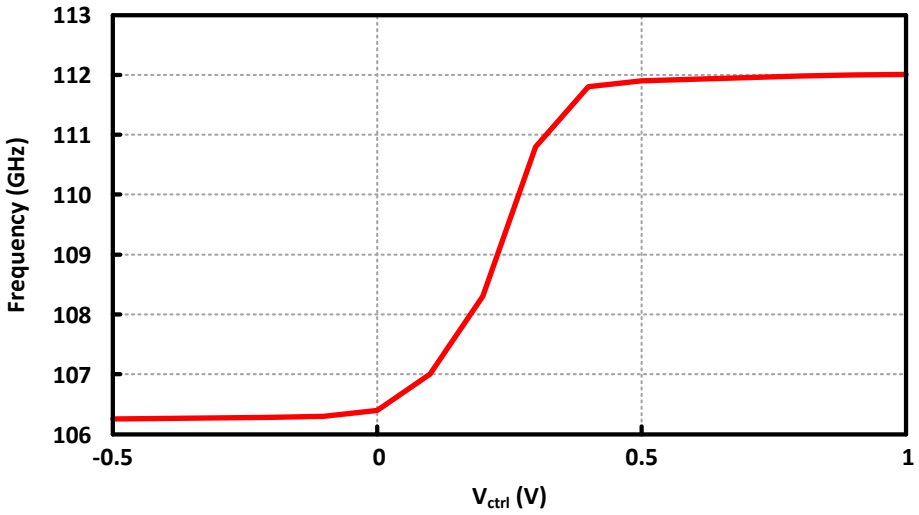

Figure 4.9: Tuning range of the designed VCO in a 55 nm SiGe process

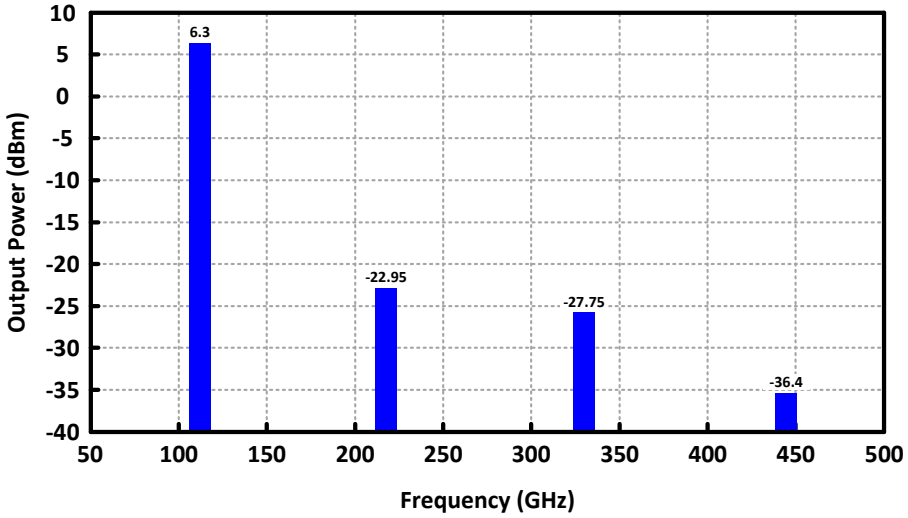

Figure 4.10: Peak output power of the designed VCO in a 55 nm SiGe process

4.5 Conclusion

A systematic method for efficient mm-wave VCO design is presented. Using the proposed structure and the oscillator power gain ($G_{p,osc}$), an optimization problem in terms of the y-parameters of the transistor and the embeddings and load is defined. Solving this problem in SNOPT as optimization solver, the optimum embeddings and the load are provided. A 110 GHz VCO is realized in a 55 nm SiGe process to justify the approach. The designed VCO achieves 6.3 dBm output power and 20.9% DC-to-RF efficiency. The frequency can be changed from 106.4 GHz to 112 GHz which results in 5.2% tuning range. This VCO achieves highest peak output power in F and D band and highest DC-to-RF efficiency below $f_{max}/2$ among all mm-wave VCO's in SiGe/CMOS processes.

Table 4.1: Comparison Table

	Technology	**Frequency (GHz)**	**Output Power (dBm)**	P_{dc} **(mw)**	**DC-to-RF Efficiency (%)**	**Tuning Range (%)**
[102]	65 nm CMOS	98	-1	21.5	3.7	8.7
[104]	65 nm CMOS	100	-2	21	3	5.2
[94]	130 nm CMOS	104	-2.7	21	2.56	-
[105]	90 nm CMOS	104	-8.2	5.8	2.61	-
[88]	65 nm CMOS	105	4.5	54	5.22	9.5
[106]	130 nm SiGe	106	2.5	133	1.35	4
[98]	65 nm CMOS	106.7	< -15	30	0.1	39.4
[107]	210 nm SiGe	109	1	36	3.5	3.67
[100]	65 nm CMOS	115	-2.5	10.6	5.3	4.4
[101]	65 nm CMOS	118	-14	5.6	0.71	7.8
[94]	130 nm CMOS	121	-3.5	28	2.13	-
[108]	130 nm SiGe	121	1.5	42	3.36	18.2
[107]	210 nm SiGe	121	6	72	5.25	2.48
This Work	**55 nm SiGe**	**109**	**6.3**	**16.9**	**20.9**	**5.2**

CHAPTER 5

HIGH POWER AND EFFICIENCY TERAHERTZ HARMONIC OSCILLATOR

5.1 Introduction

Mm-wave and terahertz frequency range promises different applications in various areas including spectroscopy [12, 14, 109], imaging [83–85], security [86] and high data-rare communication [16, 17, 87]. Signal sources are one of the main blocks in these systems and many of them have been fabricated in SiGe and CMOS processes working beyond 0.75 f_{max} [89, 94, 110–119] to show the feasibility of implementing these systems. Despite all the efforts and ideas employed to enhance the output power and efficiency of the oscillators working close or above f_{max} of the device, there is still a long way to go to achieve reasonably high performance signal sources.

The main challenge in mm-wave and terahertz oscillator design lays in the degraded U of the device and high loss of the passives at this frequency range. In fact, as frequency increases to above $f_{max}/2$, U of the device decreases with slope of $\sim$ 20 dB/dec [20] and reaches to 1 at f_{max} after which the device is no longer active. Since U is the measure of activity of the device [6], having lower U means lower capability in power generation. In addition, high loss in passives due to skin effect and working close to their resonance frequency make it harder to achieve and extract high output power out of the oscillator [19].

In recent years, there have been significant improvements in device fabrication in SiGe and CMOS technologies which lead to higher f_{max} for the transistors [21] and help to realize sources working at terahertz frequency range, however achieving high performance oscillator at these frequencies needs deep understanding of the basics and

mechanism of power generation in the device and employing efficient ways to extract it completely. In general, there are two main approaches to design terahertz signal sources: oscillators that deliver power to the load at the fundamental frequency and sources in which the power is extracted at one of the harmonics.

In the first category, the operation frequency is theoretically limited to below f_{max} of the active device, however, in practice achieving high performance beyond 0.75 f_{max} is a hard goal to achieve due to significantly degraded U of the active device. Many of the reported fundamental oscillators have utilized known structures like Colpitts, cross-coupled or ring as the general topology with changes in some parts of the circuit in order to enhance the performance [20, 93, 111, 120, 121]. On the other hand, in some works the main effort is to define a function related to the generated power or activity of the device which maximizing it helps to increase output power and efficiency. In [63], maximally efficient power gain is maximized at the operation frequency to enhance power gain and efficiency. In [19], U of the structure as the activity measure is maximized and shaped using optimum embeddings to achieve this goal. The optimum values to maximize $\frac{P_R}{|V_{in}||V_{out}|}$ was utilized in [94] to have high output power oscillator at fundamental frequency.

The idea in second approach is to extract power at one of the harmonic frequencies to have higher operation frequency which can go beyond f_{max} of the process. This is one of the significant advantages of this approach over the first one. In most works, the effort is to design a high power fundamental oscillator and hope that higher power at the fundamental leads to higher power at the harmonics [92, 94, 95]. However, the generated power at the desired harmonic frequency in these oscillators is not sufficiently high. Therefore, a common way to have higher output power at high frequencies is utilizing array of coupled sources and combining their output power

[89, 110, 113, 114, 116–119, 122, 123]. Although this method is beneficial to provide sufficient output power, but it significantly increases dc power consumption which increase the heat generation in the die and hence requires a cooling system to alleviate this issue. Moreover, due to the added passive components in the system, loss of the circuit increases which results in degradation in Dc-to-RF efficiency. In addition, the occupied area increase considerably which leads to higher cost and an obstacle for industrializing the idea and implementing small portable THz devices. In fact, the high output power is achieved in price of degrading power-area efficiency of the work drastically. The highest output power and DC-to-RF efficiency among signal sources in SiGe and CMOS working beyond 0.75 f_{max} is achieved in [116] employing this technique which shows 5.4 dBm output power and 5.15% efficiency at 296 GHz in a 65 nm CMOS process. This work utilizes a 2×3 array of oscillators occupying 2.22 mm^2 silicon area which results in 1.56 mW/mm^2 power-area efficiency.

In section 5.2, a systematic method for high output power single harmonic oscillator design is proposed which results in significantly high power to area efficiency. A design example is presented in section 5.3 in which based on the proposed method, a 300 GHz harmonic oscillator is designed which achieves 2.8 dBm output power and 4.5 % DC-to-RF efficiency while the core oscillator occupies only 0.022 mm^2 which results in record power-area efficiency of 86.6 mW/mm^2. the conclusion part summarizes this chapter.

5.2 Proposed Method

In the harmonic oscillator design, there are three main factors to work on in order to have high harmonic generation. First, having a well-designed and high power fundamental efficiency can help to have higher power at harmonics and this strategy has been used

in many works to have power at harmonic frequency [92, 94, 95]. The other important factor is to design a circuit which is capable of harmonic generation which is a product of nonlinearity. This approach has not been studied profoundly since it is totally a nonlinear process and linear methods cannot capture this effect. Last but not least, a mechanism to fully extract the generated harmonic power at the output is required to successfully achieve the goal of high power extraction at the output.

In this section, a novel method for designing high power harmonic oscillator using cross-coupled structure is proposed. It exploits different mechanisms to achieve high power generation at the desired harmonic. First, a high power fundamental oscillator is designed employing capacitive degeneration to boost and shape the G_{out} of the structure which is desired to be most negative at the fundamental oscillation frequency. Second, an inductive embedding is utilized to increase the voltage gain from output to the input of the transistor. This results in large voltage swing at this port of the transistor and hence increasing the capability of the device in harmonic generation significantly. At the final stage, the matching at the output is done using proper embeddings to fully extract the generated power at the second harmonic. In the following parts, these ideas are explained completely.

5.2.1 G_{out} Boosting Structure

Before explaining the main idea, it is beneficial to note that a two-port network can be modeled in terms of embeddings and dependent current sources as depicted in Fig. 5.1 using its y-parameters. Since this representation is a general form, it is helpful to define Y_{out} of a cross-coupled structure utilizing this model for each active core to gain insight toward design process.

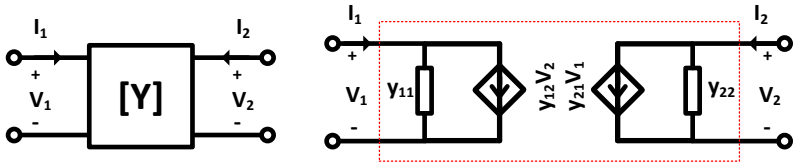

Figure 5.1: Representation of a two-port network as a circuit model using its y-parameters

Assume a cross-coupled structure as shown in Fig. 5.2 in which two identical active devices are replaced by their circuit model representation. The output admittance of the structure can be found using the setup depicted in right side of Fig. 5.2 as:

$$Y_{out,conv} = -\frac{y_{21} + y_{12}}{2} + \frac{y_{11} + y_{22}}{2}. \tag{5.1}$$

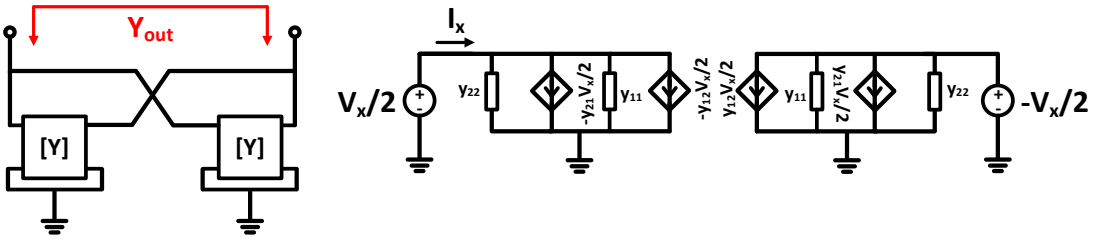

Figure 5.2: Left: A cross-coupled structure Right: The setup for finding Y_{out} using circuit model representation of active devices

At the oscillation frequency, the real part of Y_{out}, i.e. G_{out}, should be negative to provide energy to the resistive load and compensate loss of the circuit while the imaginary part of that should be resonated out connecting porer reactance to the circuit. Having more negative G_{out} means the oscillator can compensate more loss and tolerate smaller load and is capable of giving more power to the output. A conventional cross-coupled oscillator employs simple transistor as its active core. In order to calculate G_{out} of this

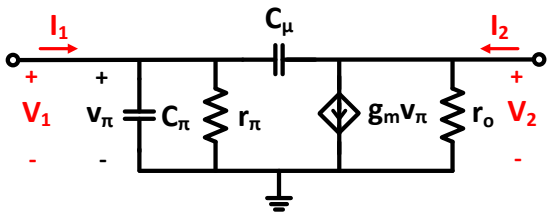

Figure 5.3: The transistor model employed to derive its y-parameters

structure, the y-parameters of a simple transistor is needed. Using the definition of y-parameters and the transistor model shown in Fig. 5.3, each component of y-matrix can be derived:

$$\begin{aligned} y_{11} &= \tfrac{1}{r_\pi} + (C_\pi + C_\mu)s. \\ y_{12} &= -C_\mu s. \\ y_{21} &= g_m - C_\mu s. \\ y_{22} &= \tfrac{1}{r_o} + C_\mu s. \end{aligned} \tag{5.2}$$

Substituting these values into (5.1) and considering the real part of that results in the known real part of output admittance of a conventional cross coupled structure:

$$G_{out} = -\frac{g_m}{2} + \frac{1}{2r_o} + \frac{1}{2r_\pi}. \tag{5.3}$$

As it is evident from (5.3), the value of G_{out} in conventional cross-coupled is a strong function of g_m of the transistor which drastically drops as frequency increases. This means as frequency goes higher, the transistor capability in providing negative G_{out} in a conventional cross-coupled degrades and at some point it is no longer capable of introducing negative G_{out}. In order to have oscillation at higher frequency, the designer has to increase g_m which is usually done by increasing dc power and degrading the efficiency.

In order to have a mechanism to control G_{out} effectively and make it negative especially at high frequencies, the structure depicted in Fig. 5.4 is proposed in which a capac-

itive embedding is connected to the emitter of the transistor. To analyze its functionality, first consider the general combination of transistor and an embedding connected to its emitter as new active core as shown in Fig. 5.4.

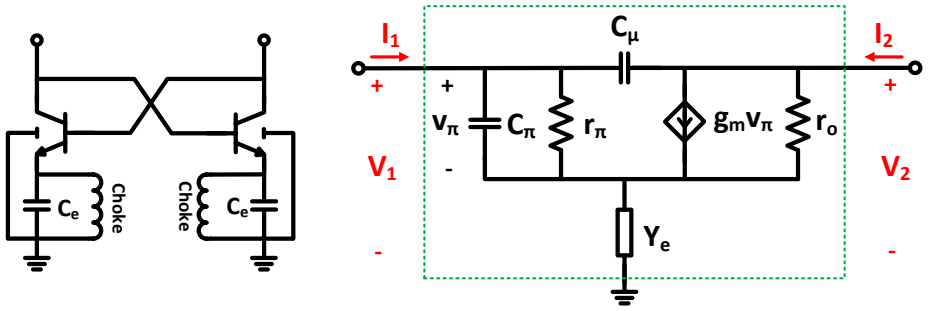

Figure 5.4: Left: Capacitive degenerated cross-coupled Right: The degenerated transistor model to derive y-parameters

To derive Y_{out} of the cross-coupled structure utilizing this combination as the active device, the y-parameters of the network should be written. Using the definition of y-parameters and the model shown in Fig. 5.4, the y-parameters can be written as:

$$\begin{aligned}
y_{11} &= \frac{(\frac{1}{r_\pi}+C_\pi s)(\frac{1}{r_o}+Y_e)}{g_m+\frac{1}{r_o}+\frac{1}{r_\pi}+C_\pi s+Y_e} + C_\mu s. \\
y_{12} &= -\frac{(\frac{1}{r_\pi}+C_\mu s)\frac{1}{r_o}}{g_m+\frac{1}{r_o}+\frac{1}{r_\pi}+C_\pi s+Y_e} - C_\mu s. \\
y_{21} &= \frac{(\frac{1}{r_o}+Y_e)(\frac{1}{r_o}+g_m)}{g_m+\frac{1}{r_o}+\frac{1}{r_\pi}+C_\pi s+Y_e} - \frac{1}{r_o} - C_\mu s. \\
y_{22} &= -\frac{(\frac{1}{r_o}+g_m)\frac{1}{r_o}}{g_m+\frac{1}{r_o}+\frac{1}{r_\pi}+C_\pi s+Y_e} + C_\mu s + \frac{1}{r_o}.
\end{aligned} \tag{5.4}$$

Y_{out} of the degenerated cross-coupled is calculated by substituting (5.4) in (5.1) which results is:

$$Y_{out} = \frac{1}{r_o} + 2C_\mu s + \frac{1}{2}\frac{(C_\pi(Y_e+\frac{1}{r_o})+C_\mu\frac{1}{r_o})s + (Y_e+\frac{2}{r_o})(\frac{1}{r_\pi}-\frac{1}{r_o}-g_m)}{g_m+\frac{1}{r_o}+\frac{1}{r_\pi}+C_\pi s+Y_e}. \tag{5.5}$$

Since Y_e is a frequency dependent admittance, its type and value greatly impacts the real part of the Y_{out}. Indeed, using a capacitive Y_e results in totally different fractional

compared to inductive Y_e. Assuming $Y_e = C_e s$, the output admittance would be:

$$Y_{out,C_e} = \frac{1}{r_o} + 2C_\mu s + \frac{1}{2}\frac{C_\pi C_e s^2 + (\frac{(C_\pi+C_\mu)}{r_o} + C_e(\frac{1}{r_\pi} - \frac{1}{r_o} - g_m))s + \frac{2}{r_o}(\frac{1}{r_\pi} - \frac{1}{r_o} - g_m)}{g_m + \frac{1}{r_o} + \frac{1}{r_\pi} + (C_e + C_\pi)s}. \quad (5.6)$$

while connecting an inductive $Y_e = \frac{1}{L_e s}$ yields to a different equation for Y_{out}:

$$Y_{out,L_e} = \frac{1}{r_o} + 2C_\mu s + \frac{1}{2}\frac{(C_\pi + C_\mu)\frac{L_e}{r_o}s^2 + (C_\pi - 2L_e(\frac{g_m}{r_o} + \frac{1}{r_o^2} - \frac{1}{r_o r_\pi}))s + (\frac{1}{r_\pi} - \frac{1}{r_o} - g_m)}{L_e C_\pi s^2 + L_e(g_m + \frac{1}{r_o} + \frac{1}{r_\pi})s + 1}. \quad (5.7)$$

Figure 5.5 shows real parts of Y_{out,C_e} and Y_{out,C_e} derived in (5.6) and (5.7) using transistor model assuming $g_m = 20m$, $r_\pi = 500\Omega$, $r_o = 2k\Omega$, $C_\pi = 40fF$ and $C_\mu = 15fF$ employing $C_e = 30fF$ and $L_e = 50pH$ which clearly shows the different behavior of these two degeneration types.

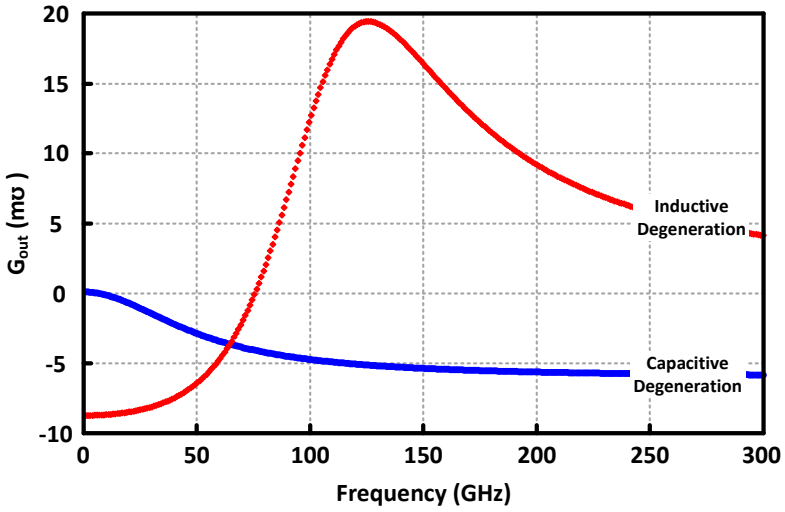

Figure 5.5: G_{out} for a cross-coupled structure with capacitive and inductive degeneration using high frequency transistor model

Figure 5.6 shows G_{out} using PDK models of the transistors provided by the foundry for the conventional and degenerated cross-coupled structure employing two transistors with 2×3 μm emitter length biased at 6.3 mA collector current in a 130 nm SiGe

process which demonstrates almost the same behavior using the derived equations. As it is evident form these two plots, using an inductive degeneration embedding degrades G_{out} of the structure at all frequencies whereas capacitive one can enhance and shape it at the desired frequency by choosing proper value for C_e.

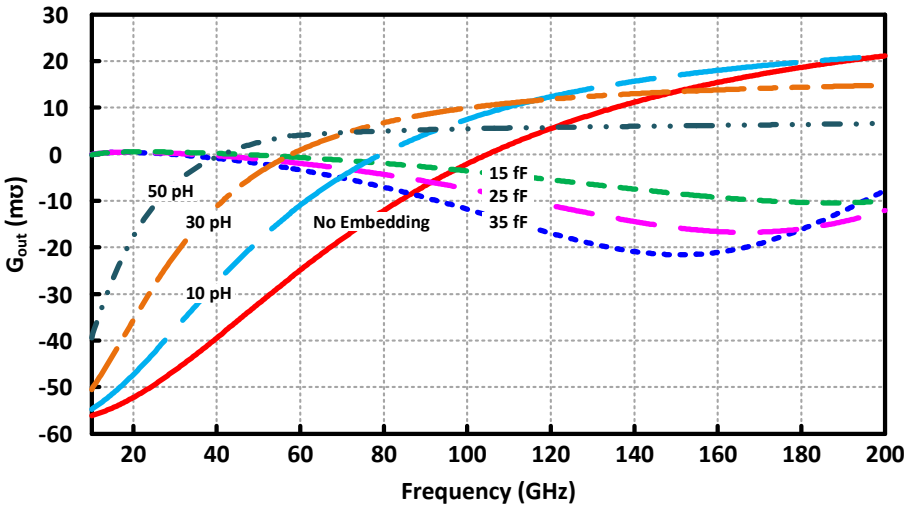

Figure 5.6: G_{out} of the conventional and degenerated cross-coupled structure for different values of C_e and L_e employing $2 \times 3\ \mu m$ transistors in a 130 nm SiGe process

In fact, C_e can be chosen such that G_{out} of the structure becomes a large negative quantity at high frequency. Therefore, employing the capacitive degeneration in cross-coupled structure as proposed, provides the degree of freedom to control G_{out} of the oscillator and make it most negative at the desired frequency. In addition, this structure has a great advantage for pushing the oscillation frequency to higher ranges. In fact, as shown in Fig. 5.6, the conventional cross-coupled structure employing the same transistor bias and size cannot be used as the active core of an oscillator for frequencies above $\sim$ 100 GHz since its G_{out} becomes positive whereas G_{out} in the proposed structure can be made most negative at the desired frequency just by setting the proper value for C_e. This means utilizing the proposed structure, the same transistor with the same bias

can be used as the active core of the oscillator at frequencies higher than 100 GHz.

Examining (5.6) shows that as C_e increases, G_{out} acquires its most negative point at lower frequencies. The extreme case is when C_e becomes infinity. In this case, as can be seen from (5.6), G_{out} becomes equal to value derived for simple transistor in 5.3. This is expected by intuition too, since very large C_e means having no embedding at the emitter which is equivalent to the conventional structure.

5.2.2 Harmonic Generation Embedding

Designing a high power fundamental oscillator and extracting the generated harmonic power is a common method to have a harmonic oscillator. However, having high power at the fundamental does not necessarily result in efficient harmonic power generation. Therefore, in order to further enhance output power at harmonic frequencies, a mechanism for generating power at the harmonics is required.

Harmonic generation is a product of nonlinearity in the circuit. Therefore, to generate higher power at the harmonic frequencies, the nonlinearity of the device should be utilized. Both BJT and CMOS transistors show nonlinearity as the signal at their input port becomes large signal. This behavior is stronger in SiGe transistors since the I-V curve is an exponential function and rich in harmonic contents when the device is excited by large input voltage. Therefore, the idea is to find a way to feed the transistor with high swing voltage which results in generating high harmonic current at the output of the device.

Assume the general form of a cross-coupled as shown in Fig. 5.2. In this structure, the input of each device is directly connected to one of the outputs and follows the

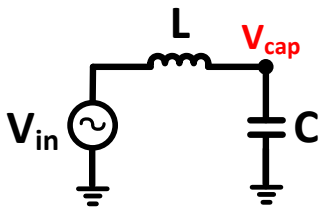

Figure 5.7: A series LC circuit excited by a sinusoidal voltage source

signal at that node. In order to increase the voltage swing at the input of the active core, a method that provides voltage gain from output to the input is needed. To explain the concept of the idea to achieve this goal, consider an inductor and capacitor connected together as shown in Fig. 5.7. If this combination is derived by a sinusoidal voltage source as demonstrated in the figure, then the voltage at the middle node would be:

$$V_{cap} = \frac{1}{1 + LCs^2} V_{in}. \tag{5.8}$$

This equation shows that the magnitude of V_{cap} can be larger than V_{in} since the circuit has a resonance frequency ($f_{resonance}$). Figure 5.8 demonstrates this fact for a constant capacitor of value 10 fF while the value of inductor is changing from 20 pH to 50 pH which results in different $f_{resonance}$ and hence different voltage gain at desired frequency.

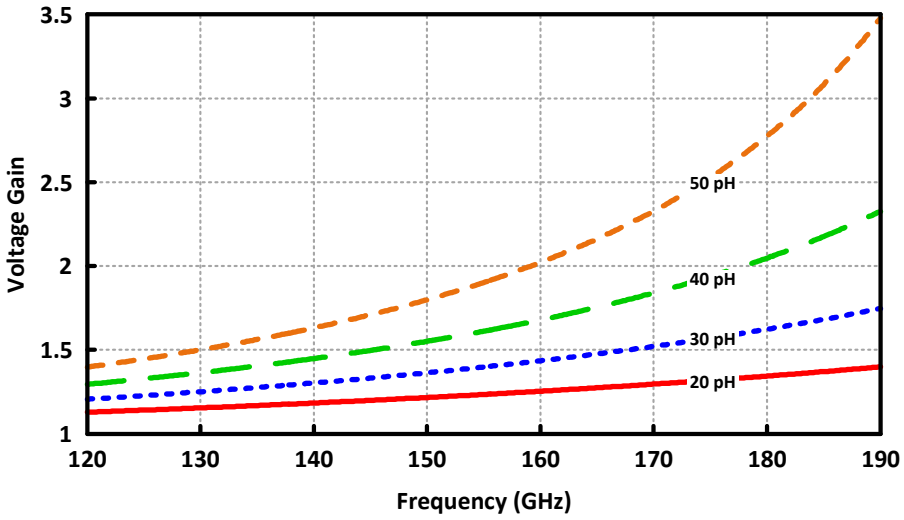

Figure 5.8: Voltage gain of a series LC circuit for different values of L and $C = 10fF$

This idea can be utilized in the proposed cross-coupled oscillator in Fig. 5.4 to increase the voltage swing at the input of the active devices with respect to the output which results in high harmonic current generation at the device. Note that the input impedance of the circuit looking into the input of the transistor is capacitive and this idea can be employed in the circuit to have voltage gain. Figure 5.9 depicts this capacitive impedance for a degenerated cross-coupled employing two 2×3 μm transistors biased at 6.3 mA collector current in a 130 nm SiGe process.

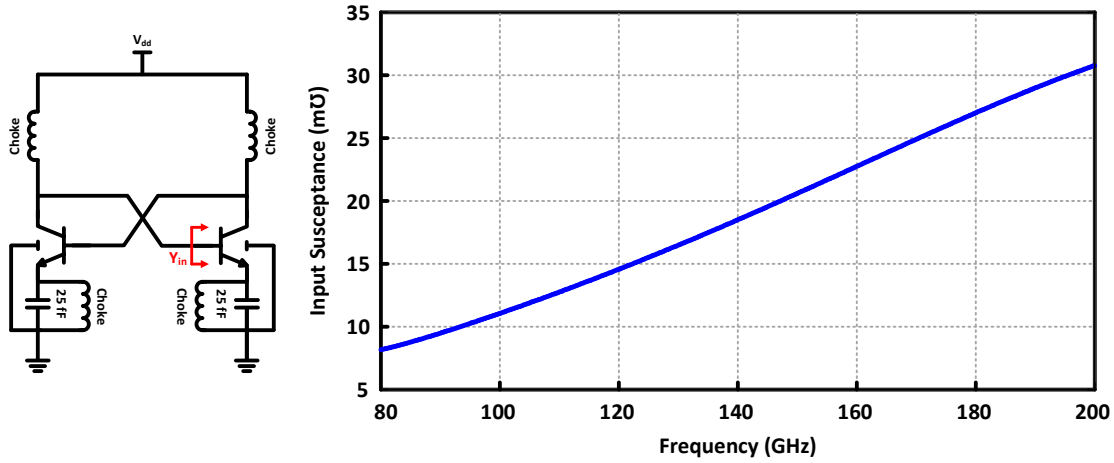

Figure 5.9: Input susceptance of the active core in the degenerated cross-coupled employing 2×3 μm transistors

Hence, utilizing an inductive impedance between the input of the device and the output node which it is connected to, as shown in Fig. 5.10, forms an LC branch in which the voltage at middle node which is the input of the device has larger swing compared to the output node and hence the conventional structure.

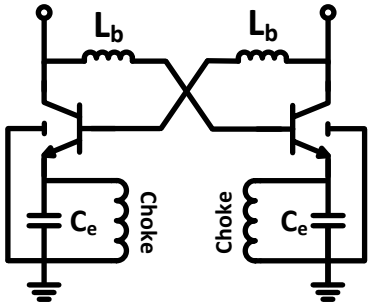

Figure 5.10: Proposed inductive embedding for boosting the harmonic generation in the structure

Possibility of having voltage gain using an inductive embedding as shown in Fig. 5.10 is demonstrated in Fig. 5.11 for this structure which employs two 2×3 μm tran-

sistors and C_e equal to 25 fF in a 130 nm SiGe process. As it is clear from this figure, selecting proper value for L_e results in large voltage gain at the desired frequency.

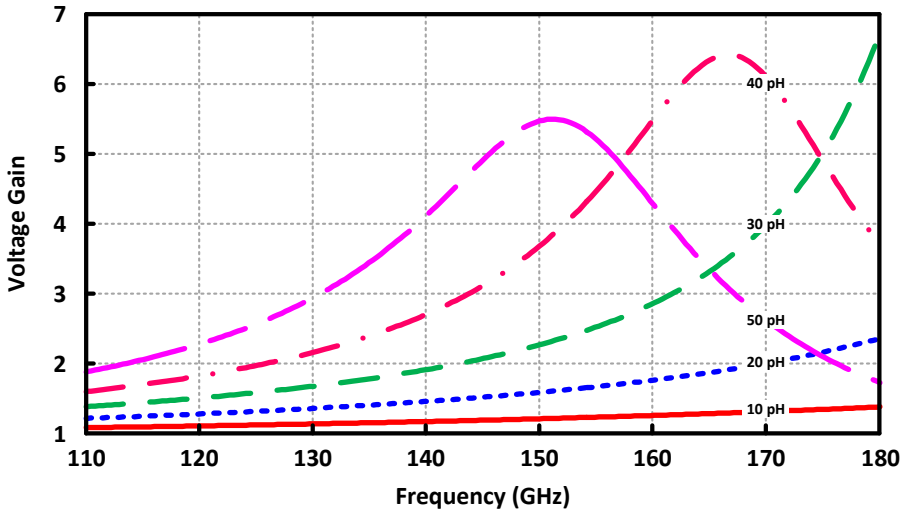

Figure 5.11: Voltage gain from inductor to the base of the transistor in the oscillator loop for different values of L_b

In order to show the efficacy of the proposed method, two capacitive degenerated cross-coupled oscillators which one of them is using L_b are designed. The first oscillator is utilizing the structure in Fig. 5.4 and the second one is employing L_b equal to 25 pH as shown in Fig. 5.10. Both oscillators are designed using ideal components and same transistor size and bias ($2 \times 3\ \mu m$ emitter length) and C_e equal to 25 fF. An ideal inductor is connected to the output nodes in each oscillator to set the oscillation frequency to 150 GHz. Figure 5.12 depicts the spectrum of the collector current in frequency which shows that the generated second harmonic current in the active device becomes more than twice ($\sim$ 125% improvement) by utilizing the inductor as proposed.

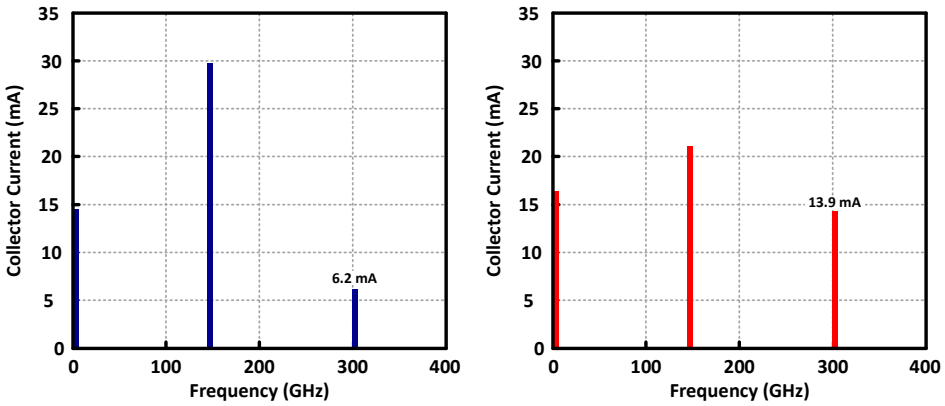

Figure 5.12: Collector current spectrum in frequency for capacitive degenerated structure without L_b (Left) and with L_b (Left)

It is worthwhile mentioning that the voltage at emitter node is a portion of voltage at the base because of the capacitive divider from base to emitter to the ground. Since the voltage difference between base and emitter (V_{be}) is important to generate effective harmonic current at the collector, the value of C_e and L_b should be chosen in a way that $A_v - \alpha > 1$ in which A_v is the voltage gain from output to the base and α is $\frac{C_\pi}{C_e}$. Employing the proposed structure, an oscillator which is rich in generating harmonic power can be achieved .

5.2.3 Efficient Output Power Extraction

The final stage of the design would be to employ a method to fully extract the generated power. To examine the real power extraction, the harmonic oscillator can be modeled as a current source containing the produced harmonic current by the active cores and a resistance as shown in Fig. 5.13 which are connected to the load.

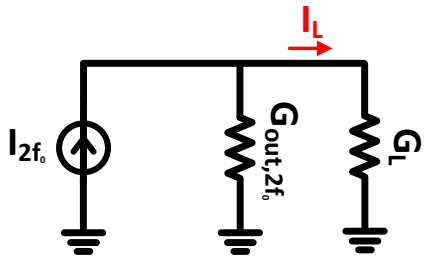

Figure 5.13: Loaded harmonic oscillator circuit model for real power extraction at the harmonic frequency

The ideal scenario to extract the most real power from the harmonic oscillator is having $G_{out,2f_0} = 0$ so that all the generated harmonic current totally flows into the load. Therefore, to extract the highest output power by the load at the desired harmonic, the output resistance of the structure from the output node should be as large as possible. In order to control this resistance an embedding (L_c) is utilized in the design as shown in Fig. 5.14 to provide enough degree of freedom to achieve this goal. An other embedding (L_{cc}) is added to the structure in order to set the oscillation frequency.

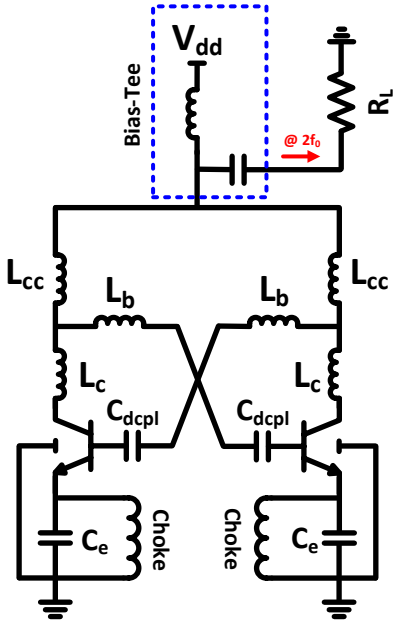

Figure 5.14: Complete structure of the proposed degenerated cross-coupled with inductive embedding

Having the complete structure, $G_{out,2f_0}$ of the circuit can be derived using the oscillator model at second harmonic as depicted in Fig. 5.15.

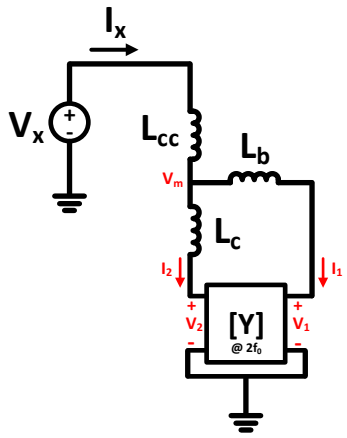

Figure 5.15: Circuit model of the oscillator at harmonic frequency to find output conductance ($G_{out,2f_0}$)

As it is shown in the following equations, L_{cc} has negligible effect on $G_{out,2f_0}$ for practical values and output resistance of the structure can be effectively set using L_c. Considering the y-parameter definition and current relations in the circuit, it is found that:

$$\begin{aligned} I_x &= V_1(y_{21}+y_{11}) + V_2(y_{12}+y_{22}) \\ V_1 &= \frac{s(L_g y_{12}-L_c y_{22})-1}{s^2 L_g L_c(y_{12}y_{21}-y_{11}y_{22})-s(L_c y_{22}+L_g y_{11})-1} V_m. \\ V_2 &= \frac{1}{1+sL_c y_{22}} V_m - \frac{sL_c y_{21}}{1+sL_c y_{22}} V_1 \end{aligned} \tag{5.9}$$

and Z_x is derived as:

$$Z_x = \frac{V_x}{I_x} = sL_{cc} + \frac{\beta(1+sL_c y_{22})}{(y_{21}+y_{11})(\alpha(1+sL_c y_{22})) + (y_{12}+y_{22})(\beta - sL_c y_{21}\alpha)}, \tag{5.10}$$

in which

$$\begin{aligned} \alpha &= L_g y_{12} - L_c y_{22} - 1 \\ \beta &= s^2 L_g L_c(y_{12}y_{21}-y_{11}y_{22}) - s(L_c y_{22}+L_g y_{11}) - 1. \end{aligned} \tag{5.11}$$

and is calculated as $G_{out,2f_0} = 0.5\frac{Re(Z_x)}{|Z_x|^2}$. It is clear from the derived equations that after choosing transistor bias and size, C_e and L_b, the output conductance of the circuit can be changed using L_c since it is a strong function of this embedding. Then the frequency can be tuned employing proper value for L_{cc} and this embedding does not change output conductance significantly. Indeed, these two embeddings are inevitable when laying out the circuit, hence considering them in the design process achieves two goals. First, the effect of them in the design and performance of the circuit is captured as part of the design. Second, they can be selected in the way to help enhancing the performance of the circuit rather than a mandatory parts forced by the layout which usually degrade the performance.

In the design process, following the main guidelines for each component considering its role results in high power and efficiency harmonic oscillator at second harmonic. In

the next section, a design example is presented and these details are discussed to achieve an efficient 300 GHz harmonic oscillator employing the proposed structure.

5.3 Design Example: 300 GHz Harmonic Oscillator

In this section, employing the proposed structure, a harmonic oscillator and a VCO at 300 GHz in a 130 nm SiGe process are designed. The harmonic oscillator shows 2.8 dBm peak output power and 4.5% best DC-to-RF efficiency at 300 GHz. The harmonic VCO has 2.3 dBm peak output power, 3.5% best DC-to-RF efficiency and 1.5% tuning range with center frequency at 295 GHz.

5.3.1 Passives and Transistor Bias and Size Selection

The first step to start the design is choosing transistor size and bias. This selection should be done wisely since the transistor is heart of power generation in the structure. A high activity transistor is desirable since it is capable of having higher power generating. The activity of a transistor can be studied by examining its U as the activity measure at the desired frequency, higher U means more active device. On the other hand, producing output power at is a strong function of dc power consumption. Therefore, for a given V_{dd} which is usually set by the process, the dc bias current has an important role in defining the output power, higher dc current means the potential to deliver higher output power to the load. Figure 5.16 shows U at 150 GHz of transistor vs. its collector bias current for different transistor size in a 130 nm process. As it is evident from this figure, there is a trade off between U and bias current.

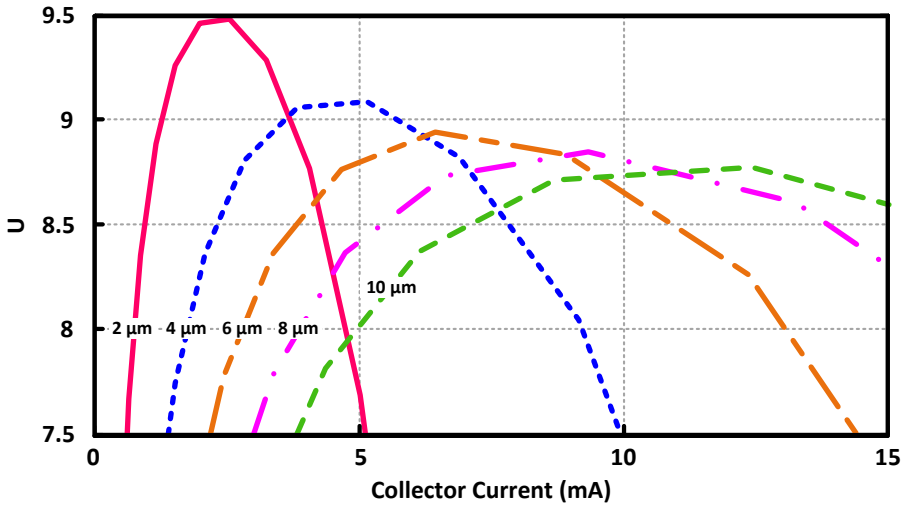

Figure 5.16: U vs. Collector bias current for transistors with different emitter lengths at 150 GHz in a 130 nm SiGe process

Higher U occurs in smaller transistor sizes and lower bias current while high bias current requires choosing larger device which its U is degraded due to higher parasitics. Therefore, based on the priorities in the design the size and bias should be selected. In this work, both high activity and high power at the output is important, hence based on the plots in Fig. 5.16, a 6 μm transistor biased at $\sim$ 6 mA is selected which its U is not degraded significantly comparing to maximum U while the dc current is sufficiently large to provide power. The number of fingers are chosen to have the highest U among all possibilities for a fixed total emitter length of 6μm that results in to have 2×3 μm transistor as the active device.

The passive structures should be selected to be able to do EM simulation and realize the actual design by replacing ideal components with real models. It is important to employ the structures that result in minimum loss so that the performance of the harmonic oscillator does not degrade drastically. Since there are different inductive embeddings in the design, a TL structure is needed to be chosen. Since the structure is a cross-coupled,

usually having walls in the TLs' makes the layout a difficult task to do. Also, for the device selected to be used in the design, the required inductive embeddings are small which means the equivalent TL has a short length and the wall cannot be employed effectively. These two facts yields in choosing simple microstrip structure. The signal track width is a significant parameter for decreasing loss and should be selected such that $\frac{\alpha}{Z_0}$ of the TL at the oscillation frequency becomes minimum [36] in which α is the real part of propagation constant and Z_0 is the impedance of the line. Therefore a microstrip with signal track width of 1.5 μm is chosen to meet this requirement. The degenerated capacitor and the ones in the matching network are realized using two-plate capacitor structure. It is using three lower metals which the middle one is sandwiched between the other two as shown in Fig. 3.19 in order to confine all the energy inside the structure and increase quality factor of the capacitor.

5.3.2 Harmonic Oscillator Implementation

After selecting the transistor bias and size, the embeddings should be found in order to boost the G_{out} of the structure and enhancing the nonlinearity of the device while resulting in the low output conductance. First, the proper C_e should be selected. Figure. 5.17 shows G_{out} for different values of C_e in a capacitive degenerated cross coupled without employing other embeddings (as depicted in Fig. 5.4).

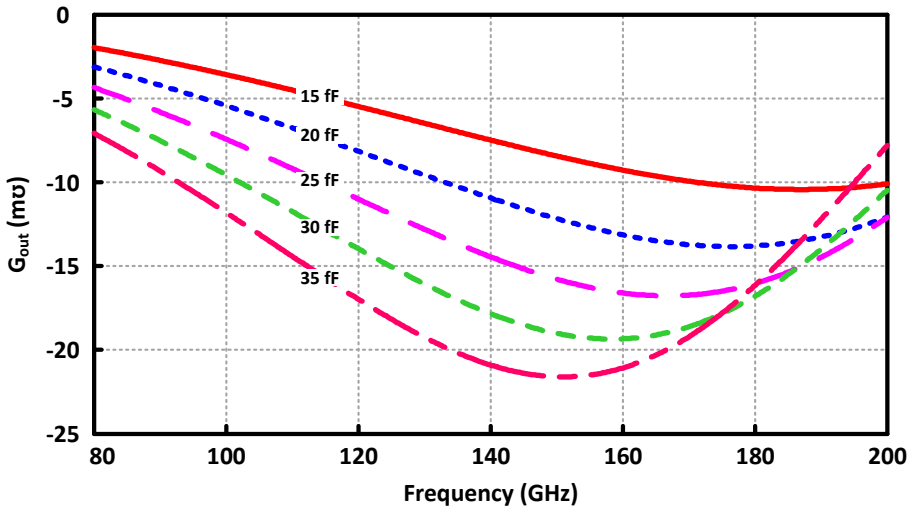

Figure 5.17: G_{out} for the capacitive degenerated cross-coupled for different values of C_e employing selected transistor size and bias

Based on this figure, the best choice of C_e for the selected transistor is 35 fF. But utilizing this value fo C_e results in a very small L_{cc} to have oscillation at the target frequency which cannot be fabricated. Therefore, smaller C_e should be selected such that practical values for all embeddings achieved. Hence, a C_e of 25 fF is chosen as the degenerated embedding. The next component to select is L_b which is done by considering the voltage devision between C_e and C_π of the transistor. In this design, C_π is $\sim$ 60 fF which means a voltage gain larger than 3 is desired. Figure 5.11, which shows A_v for the structure utilizing the selected transistor and C_e, suggests that L_b equal to 40 pH is a reasonable choice that provides the required voltage gain. Smaller value for L_b relaxes the selection of L_{cc} and results in practical values for that, so between 40 pH and 50 pH which provides larger voltage gain, the former is preferred. The value of L_c can be selected in this stage since transistor size and bias, C_e and L_b are chosen in previous steps. Selecting a L_c equal to $\sim$ 6 pH results in having a low conductance at the output of the harmonic oscillator. The last embedding which is L_{cc} can be found now since all other ones are selected. Targeting 150 GHz as oscillation frequency and considering the

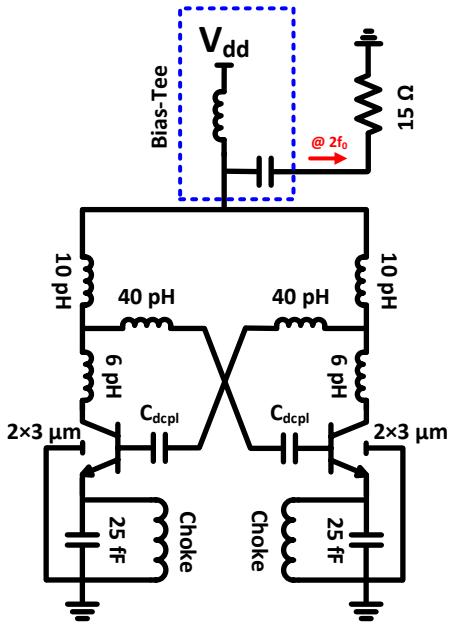

Figure 5.18: Schematic of the designed harmonic oscillator using ideal components in a 130 nm SiGe process

values selected for other embeddings, an L_{cc} of 11 pH sets the oscillation frequency of the structure to the desired one. The last stage of the design is selecting the optimum load to be connected to the output node of the structure and results in highest extracted power. A matching network at the output is required to move 50 Ω to this optimum value. The schematic of the circuit designed using ideal components are shown in Fig. 5.18. To realize the circuit using actual TL's and capacitors, the ideal components are replaced by microstrip TL's and sandwiched capacitors step by step starting from C_e and performing EM simulation for each step to minimize the effect of loss and coupling. At the final stage, the optimum load is found to be 17 Ω for the oscillator with real passives. It is worthwhile mentioning that since a capacitor is utilized in the emitter of the transistor, a $\lambda/4$ TL is used as choke to form a dc path for bias current and open circuit at the oscillation frequency. Also, a decoupling cap is designed using finger cap structure to provide sufficiently large capacitance with decent quality factor as explained in 3.6.3.

The layout of the designed harmonic oscillator is shown in Fig. 5.19. It achieves 4.5% best DC-to-RF efficiency at 303 GHz while providing 2.8 dBm peak output power as shown in Fig. 5.20. The output conductance becomes sufficiently large as depicted in Fig. 5.21 which demonstrates the efficacy of the proposed method in increasing this parameter using embeddings. The output matching is a π- network consisting of the capacitance of costume pad, a short TL and a capacitor to the ground which results in a small reflection coefficient and hence extracting the power effectively as shown in Fig. 5.22.

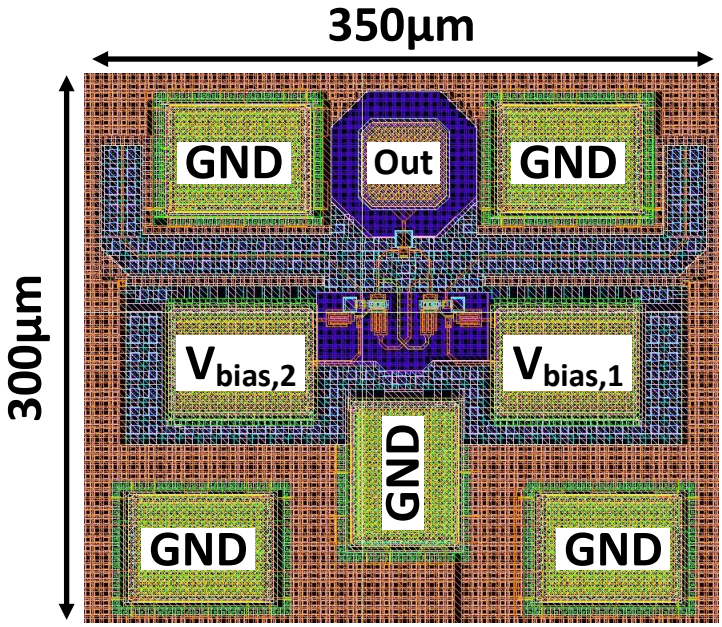

Figure 5.19: Layout of the designed harmonic oscillator in a 130 nm SiGe process

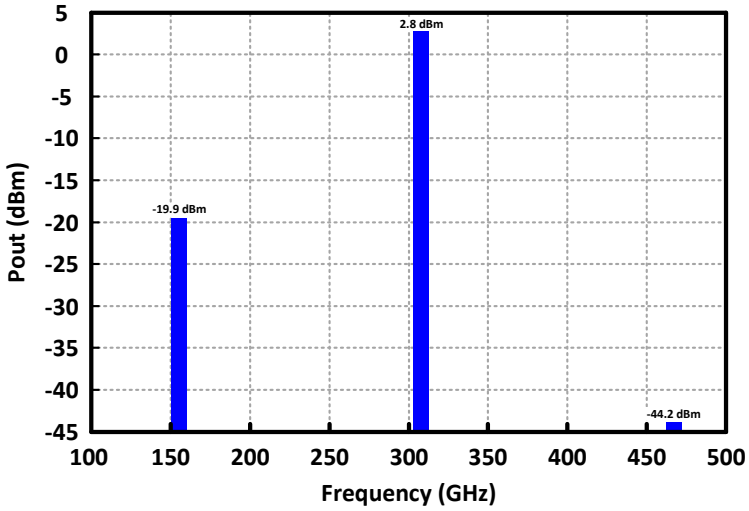

Figure 5.20: Spectrum of output power in frequency for the designed harmonic oscillator in a 130 nm SiGe process

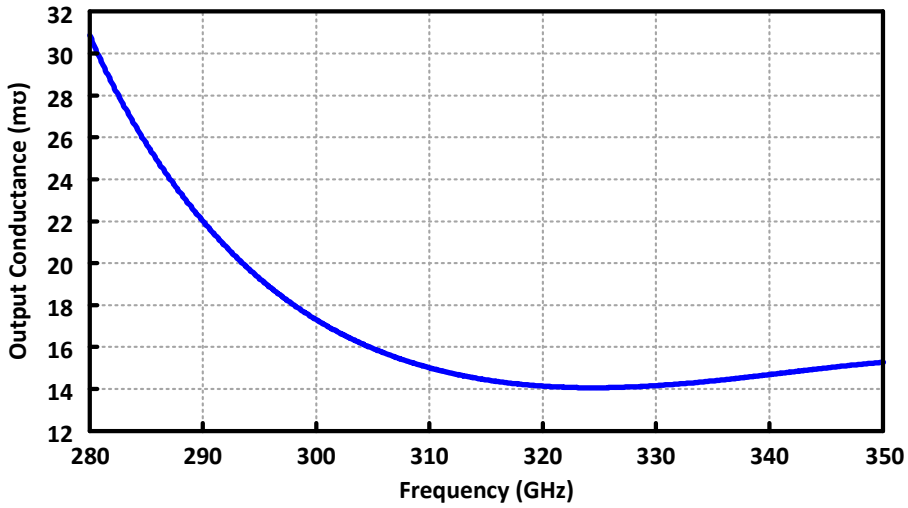

Figure 5.21: Output conductance of the designed harmonic oscillator in a 130 nm SiGe process

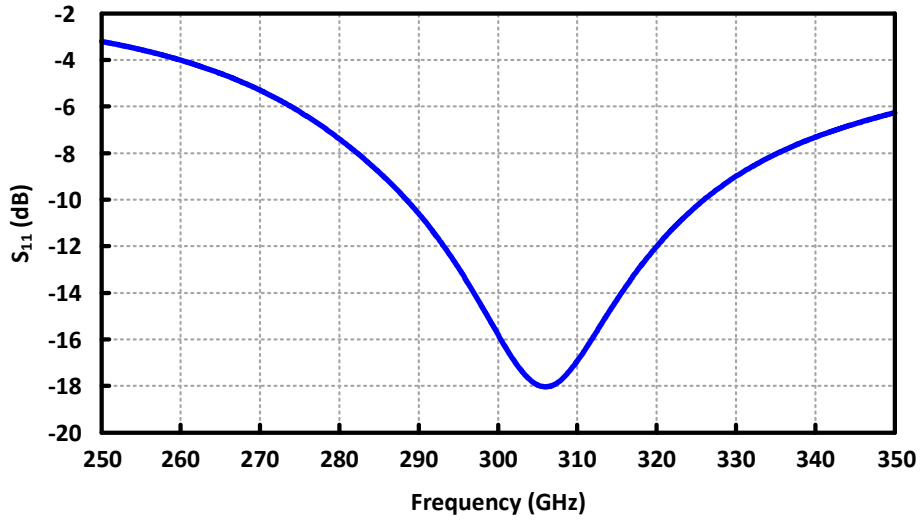

Figure 5.22: Output reflection coefficient of the designed harmonic oscillator in a 130 nm SiGe process

Using this harmonic oscillator and utilizing varactors instead of capacitor at the emitter of the transistors, a harmonic VCO is designed. Since the varactors of the process are poor in quality factor at the desired frequency, BJT's are employed to fabricate the varactors in this design. In fact, the parasitic capacitors of the transistor which are voltage dependent are used to tune the frequency. The varactor structure and specification is shown in Fig. 5.23.

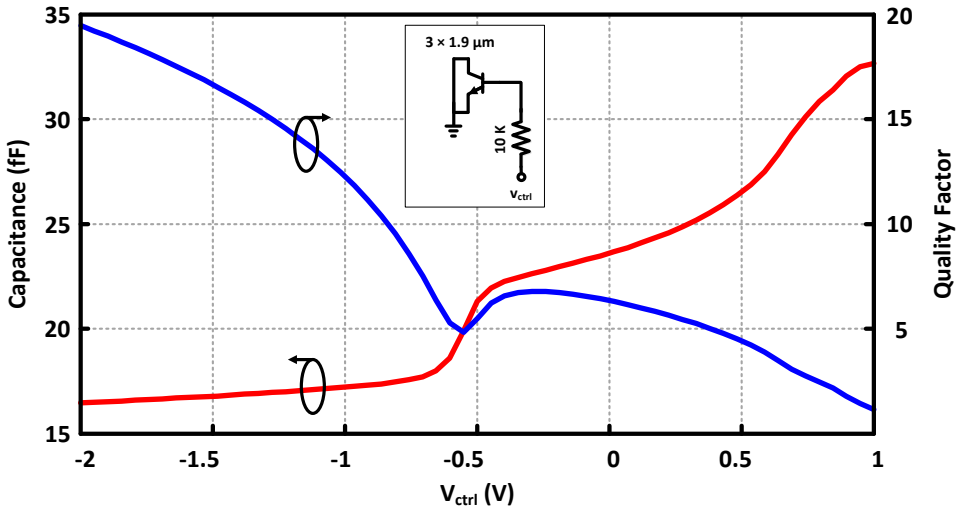

Figure 5.23: Capacitance and quality factor of a $2 \times 1.9\ \mu m$ as varactor in a 130 nm SiGe process

A decoupling capacitor is added between the varactor and the emitter to decouple the dc of this two nodes which decreases the effective capacitance since it is in series with the varactor as shown in Fig. 5.24. Employing this BJT as varactor, 1.5% tuning range with center frequency of 295 GHz is achieved which shows 3.5% best DC-to-RF efficiency and 2.3 dBm peak output power. Figure 5.26 and 5.25 depicts tuning range and output power spectrum respectively. The results of these works are compared to the state of the arts in Table 5.1 which shows that the designed single harmonic oscillator achieves highest power-area efficiency among all reported SiGe/CMOS sources working beyond 0.75 f_{max} which justifies the efficacy of the proposed method in high power generation at the desired harmonic.

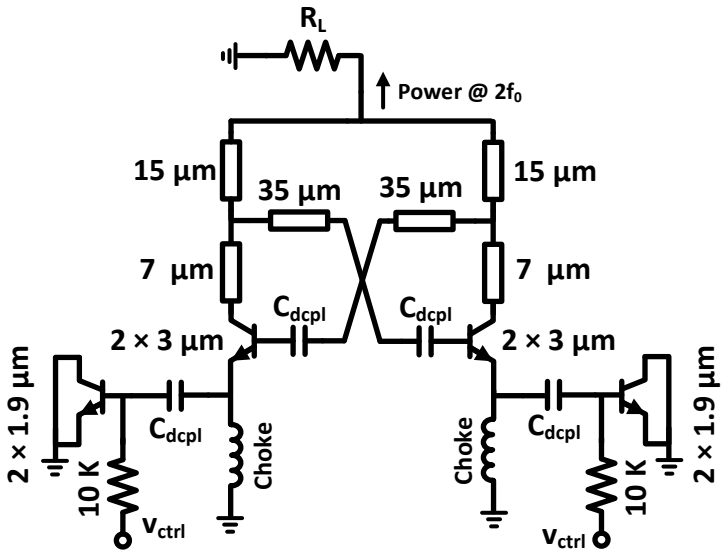

Figure 5.24: Schematic of the harmonic VCO in a 130 nm SiGe process

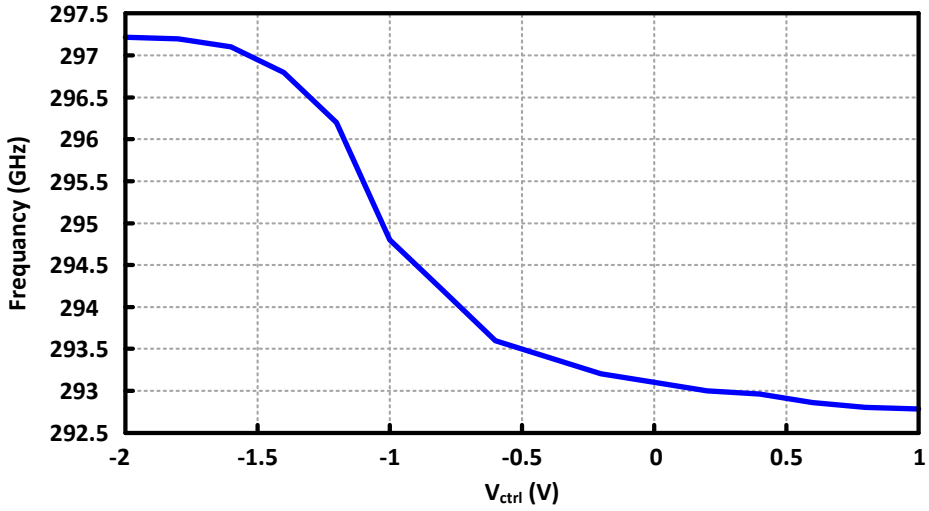

Figure 5.25: Tuning range of designed harmonic VCO in a 130 nm SiGe process

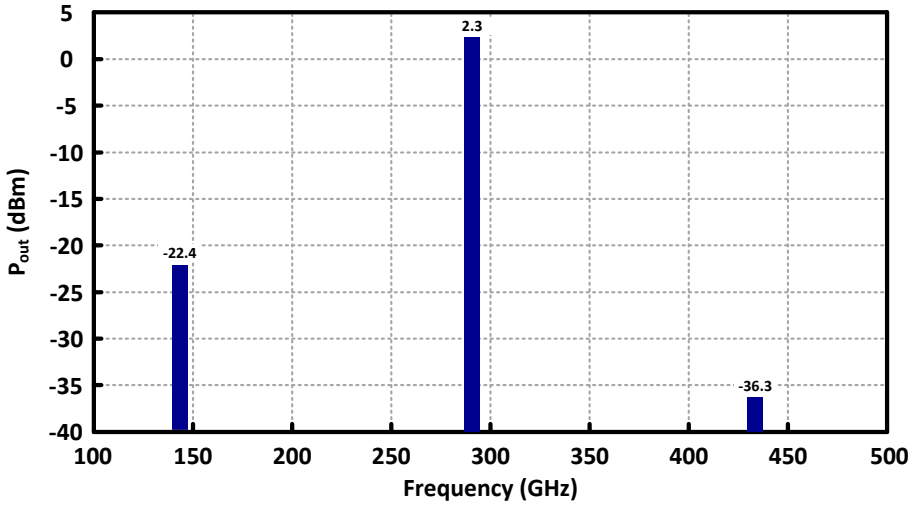

Figure 5.26: Spectrum of output power in frequency for the designed harmonic oscillator in a 130 nm SiGe process

5.4 Conclusion

In this work, a systematic method for high output power harmonic oscillator design is proposed which results in significantly high power-area efficiency. Utilizing capacitive degeneration and inductive embeddings in the structure, the capability of the oscillator in generating high output power and delivering it ot the load is enhances significantly. A design example is presented based on the proposed method, a 300 GHz harmonic oscillator is designed which achieves 2.8 dBm output power and 4.5% DC-to-RF efficiency while the core oscillator occupies only 0.022 mm^2 which results in a record power-area efficiency of 86.6 mW/mm^2 in a 130 nm SiGe process. Also, a VCO at 295 GHz with 1.5% tuning achieving 3.5% best DC-to-RF efficiency and 2.3 dBm peak output power is implemented in the same process which has 77.2 mW/mm^2 power-area efficiency.

Table 5.1: Comparison Table

	Technology	**Frequency (GHz)**	**Output Power (dBm)**	P_{dc} **(mw)**	**DC-to-RF Efficiency** (%)	**Tuning Range** (%)	**Power/Area Efficiency** (mW/mm^2)
[89]	65 nm CMOS	256	4.1	227	1.14	4.3	8.1
[94]	130 nm CMOS	256	-17	71	0.03	-	0.63
[110]	65 nm CMOS	260	0.5	800	0.14	1.4	0.49
[111]	32 nm CMOS	272	-22	7	0.09	-	1.58
[112]	65 nm CMOS	288	-1.5	275	0.25	-	39.34
[113]	90 nm SiGe BiCMOS	290	-14	105.6	0.04	8	2.65
[114]	65 nm CMOS	290	-1.2	325	0.23	4.5	2.11
[115]	65 nm CMOS	293	-2.72	19.2	2.76	5.74	2
[116]	65 nm CMOS	296	5.4	67.2	5.15	2.4	1.56
[117]	65 nm CMOS	299	0.9	235	0.52	1.7	3.35
[118]	130 nm SiGe	317	5.2	610	0.54	-	3.7
[114]	65 nm CMOS	320	-3.3	339	0.13	2.6	1.3
[119]	65 nm CMOS	338	-0.9	1540	0.053	2.1	0.24
[124]	65 nm CMOS	345	1	105	1.5	1.1	1.74
This Work	**130 nm SiGe**	**300**	**2.8**	**42.3**	**4.5**	**-**	**86.6**
This Work	**130 nm SiGe**	**295**	**2.3**	**48.5**	**3.5**	**1.5**	**77.2**

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